A 10MHz-1GHz Mitigated Shunt Capacitance Hybrid LNA for Use in a Ka-Band Envelope Detector Baseband Output

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***Abstract*—A simulated hybrid LNA exhibiting over 45 dB of power gain and <2 dB noise figure from 10 MHz to 1 GHz is designed as a baseband amplification stage for a zero-bias diode envelope detector in on-off-keying systems. The high source impedance of the diode requires mitigation and compensation of parasitic shunt capacitance between the detector and first gain stage. Here, we remove the ground plane between the first transistor stage and the diode output, as well as increasing pad-to-pad and pad-to-via spacing to reduce on-PCB parasitic shunt capacitance. The transistors are low-C_{gs} HEMTs to further ensure low shunt-capacitance to ground. We also employ inductive peaking to compensate for the dominant pole caused by the source shunt capacitance. The amplifier is expected to dissipate 8 mW from a 0.5 V source.**

I. Introduction

Massive MIMO promises to enable high-spatial-diversity high efficiency communication networks but requires hundreds to thousands of operating antennas [1]. To enable this from a hardware perspective, most commercial and academic entities are turning to power-hungry phased array solutions, while maintaining high-order, high-linearity OFDM modulation schemes. However, an alternate possible solution to the required hardware proliferation, which can address per-element power and linearity limitations of the phased array approach, is low-resolution (even 1-bit) signalling such as on-off-keying (OOK). Since ADC power consumption scales exponentially with number of bits [2] and simplification of the modulation format will relax linearity requirements [3], it is possible that millimeterwave OOK Massive MIMO networks will have an edge against conventional linear systems in a bits/Joule sense.

Schottky-diode-based envelope detectors are one potential hardware implementation of a low-power OOK receiver, which particularly can avoid inefficient LO generation and distribution, especially at millimeterwave frequencies. However, one of the principal drawbacks of the Schottky diode detector is its high conversion loss, as it is not being pumped with a high-power LO. Since the current responsivity of ideal Schottky diodes is a constant with respect to the linearized diode resistance, or video resistance R_v, [4], the voltage conversion efficiency can be increased by increasing the video resistance. However, with a higher video resistance on the order of kilohms, it is very difficult to extract the available baseband voltage from the diode (as represented by its Thévenin equivalent). This is especially true with the wide (GHz) bandwidths required for high-data rate applications employing OOK signalling, as resonant matching solutions are impractical. This work demonstrates the design and simulation of a wideband LNA for the baseband output of such a high-impedance Schottky-diode envelope detector.

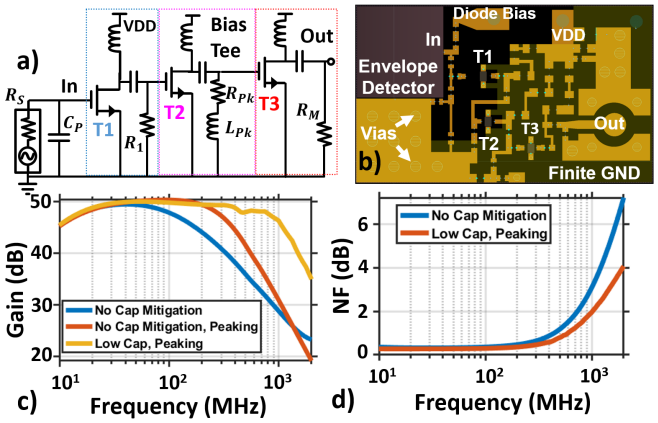

Fig. 1. a) A simplified circuit model of the amplifier. R_1 is greater than $1\,k\Omega$, R_{Pk} and R_M are $75\,\Omega$, L_{Pk} is around 100 nH, and the tee inductance is $2.7\,uH$. b) The proposed layout, with removed ground plane around transistor T1. The transistor locations are denoted by T1, T2, and T3, where there are through vias to the backside ground, to which the transistor sources are wirebonded. The layout additionally has a diode DC bias path for bias-dependent measurement of the envelope detector. c) The layout alterations show a clear improvement in the high-band gain due to shunt capacitance mitigation. In the absence of these alterations, shunt peaking alone shows a substantial (almost 2x) improvement in $3\,dB$ bandwidth. The high power gain demonstrated is heavily due to the impedance transformation from the $2\,k\Omega$ source to $50\,\Omega$ load. d) The LNA exhibits good noise performance across the band of interest (up to 1 GHz).

II. Design

The proposed broadband LNA consists of three cascaded common-source InP HEMT transistors, using the pH-100-2F25 equivalent circuit model provided by Diramics [5] (Fig.

1a). The cascaded topology allows for low drain voltage (0.5V), while providing high gain of up to 35 V/V within the band (with an average voltage gain of 27 V/V). The transistors are especially attractive in this application for their low C_{gs} of 40 fF, low power dissipation (2 mW at $V_{ds} = 0.5\,V, V_{gs} = 0\,V$, and high transconductance. Each transistor stage accomplishes a different primary purpose in the cascade. The first stage (T1) has a high impedance resistive load such that its gain approaches the pH-100-2F25 intrinsic gain. The transistors have a drain-source resistance of $r_o \approx 240\Omega$ and transconductance of $g_m \approx 54\ mS$, giving an intrinsic gain of 13 V/V. The second stage (T2) has a series R-L load, which sacrifices achievable gain at the low end of the band to insert a transfer function zero compensating for the single pole behavior of the input parasitic capacitance (shunt peaking). Pads for a resistor are placed in parallel with the inductor to de-Q any resonances that arise after fabrication. The purpose of T3 is to transform the output impedance to $50\,\Omega$ for interface with laboratory equipment, while providing an additional 4 V/V of gain.

Since the transistors operate in the depletion mode, the load on each transistor acts as a pull-down resistor for the gate of the next stage, ensuring proper biasing ($v_{gs} \approx 0\,V$). This is why there is a resistive load, $R_1 > r_o$ connected to T1. Power consumption is expected to increase above 6 mW from bias shift due to from parasitic drain-gate conductance at transistor T1, possible to 8 mW. The drain biasing networks are purely inductive to limit DC power dissipation. Since the transistor stages are AC coupled, the DC bias current cannot flow through the resistive loads and is almost exclusively dissipated in the transistors. SMD 0201 pads are put in series with gate and drain of T1 and T3 to for the purpose of inserting stabilizing resistors, which are of particular concern due to the high device transition frequency $f_T > 200\,GHz$.

Fig. 1b shows the resulting layout, with a substrate of 60-mil Rogers 5880 (ϵ_r = 2.2) to reduce capacitive coupling. The board measures approximately 17 mm x 10 mm, with over half of the area reserved for the envelope detector chip, bias jumpers, and an MMCX surface mount connector. The traces are electrically small and should be considered as parasitic lumped elements, not transmission lines. The region in the top left represents a $500\,\mu m$-deep milled pocket for a CPW-mounted Ka-band envelope detector in high-resistivity Si, which is demonstrated in [6]. The ground plane has been pulled back from the input network to reduce shunt capacitance, although the ground plane still reaches the transistor source vias, to which the bare die transistor will be wirebonded. Pad spacing is relatively large to mitigate edge-to-edge capacitance, especially from the bond pad to the transistor via pads. Since the input impedance of both the transistor and diode are so high $|Z| > 2\,k\Omega$, both parasitic series inductance and resistance are of lesser concern. As a result, relatively long wirebonds can be tolerated.

III. Simulation

The designed layout was simulated in the FEM tool provided in Keysight ADS, and the full circuit performance was obtained through cosimulation of the layout, vendor S-Parameters where available, and equivalent circuit models of the transistors and other SMD models. A 2 $k\Omega$ and 300 fF on-chip shunt parasitic capacitance were assumed as a realistic 'worst-case' source impedance, taking into account estimated parasitic CPW capacitance as well as a linearized circuit model of a Virginia Diodes W-band zero bias diode [7]. Notably, this produces a first-order cutoff frequency of only 265 MHz. Bondwires were modeled with equivalent series inductances and resistances. Fig. 1c shows a comparison of the proposed amplifier performance with and without inductive peaking and layout capacitance mitigation. It clearly demonstrates the high importance of layout effects on the performance near 1 GHz. This sensitivity is due to the high source impedance. The low-frequency gain droop is due to the finite bias tee inductance, and the high frequency performance is dominated by the input parasitic shunt capacitance, bias tee parasitics, and peaking response. Fig. 1d indicates the low ($< 2\,dB$) noise figure of the amplifier up to 1 GHz, owing primarily to the high noise performance of the InP HEMTs.

IV. Conclusion and Future Work

We have demonstrated here a two-decade LNA capable of high-gain and low-noise operation while terminated in a diode impedance. Amplifier performance was obtained by emphasizing the removal of shunt capacitance parasitics while accepting proportionally larger series inductive parasitics. Furthermore, inductive peaking was employed to compensate for transfer function pole caused by input RC time constant. Future work will include the fabrication and testing of the amplifier, as well as integration with the Ka-band envelope detectors mentioned herein.

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