CMOS Techniques for Communications Links beyond 100 GHz

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Recent advances in deep-sub-micron silicon technology have enabled the possibility of constructing mm-wave transceivers beyond 100 GHz in commercial CMOS technology. Such transceivers open up many new possible applications including mass data transfer kiosks, short-range high-speed interconnects, and wireless streaming of high-definition video. While CMOS dominates the commercial wireless market for popular microwave standards including (802.11a, 802.11n, 802.11ad) the roadmap for CMOS radios beyond 100 GHz is much less clear. The high levels of manufacturing variation associated with sub-micron CMOS in combination with limited transistor performance leads to limited radio reliability and low production yields. Even simple radio link issues such as frequency alignment between the transmitter, receiver, and local oscillator (LO) become more difficult. Pre-distortion and equalization also become more challenging as bandwidths for data-links beyond 100 GHz are expected to exceed 1 GB/s. Such high bandwidths put challenging design requirements on radio back-end components including baseband data-converters and subsequent digital-signal processing (DSP) for demodulation.

In this talk we will discuss several techniques employed in both 100 GHz and 144 GHz CMOS radios to alleviate the effects of manufacturing variation and restore chip yields and chip performance to an acceptable level. The solutions presented are based on real-time digital control and optimization techniques of RF circuits (power amplifiers, low noise amplifiers, and frequency synthesizers) using a variety of control circuits, sensors and signal processors. Also discussed will be an approach for backend demodulation and equalization of wide-band single-carrier modulated data-links using frequency-domain equalization techniques.