

Digital Backend Development for Bustling Universe Radio Survey Telescope (BURSTT) in Taiwan

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Abstract— We have successfully deployed and commissioned the antenna array named “The Bustling Universe Radio Survey Telescope in Taiwan” (BURSTT) at Fushan and Nantou sites for searching for fast radio bursts (FRBs). Both sites are located in Taiwan. We installed a system of 256 antennas at the Fushan main station and 64 antennas at the Nantou outrigger station. The system is composed of frontend analog microwave circuits, field programmable gate array (FPGA) as the channelizer, and a CPU-only server for processing the data. We employed the Xilinx/AMD radio frequency system on chip (RFSoc) ZCU216 board as the FPFA platform and dual Intel Xeon CPU computer as the server.

To increase the sensitivity of the telescope, we are planning to implement additional antennas at the main station. We have sampled the signal at 1920 MHz on the ZCU216 board without any issues, which makes the FPGA board more efficient by allowing two antennas input into one ADC.

I. CURRENT STATUS OF BURSTT

FRBs are intense bursts of radio waves that last a few milliseconds and release enormous amounts of energy, sometimes equivalent to the entire solar radiation emitted in a day. They remain one of the most mysterious and exciting phenomena in astrophysics. The most compelling reason scientists are still searching for FRBs is that their exact origin is still unknown. Despite their discovery over a decade ago [1], the mechanism that generates these bursts is still unclear. Even there are couple of telescopes dedicated for this purpose such as the CHIME (Canadian Hydrogen Intensity Mapping Experiment) [2], FAST (Five-hundred-meter Aperture Spherical Telescope) [3], square kilometer array (SKA) [4] and other modern observatories, the question remains unanswered.

BURSTT [5] project has already implemented 256 antennas array (16x16) in the main station Fushan. It is located in the Fushan Botanical Garden. Currently we are collecting real time data and waiting for trigger by FRBs. Besides the main site, an outrigger station at Nantou in the central Taiwan, 64 antennas (4x16) system is fully built and well commissioned. We are waiting for the trigger as well.

Another outrigger station is located on Green Island, a tiny island off the east coast of Taiwan. The infrastructure for 64 antennas has been completed and is waiting for the commissioning. Meanwhile, our Hilo team, on the Big Island, Hawaii has already completed the site preparation and is waiting for system implementation. Besides Taiwan, we are collaborating with Japan, India and other Asian countries to achieve a longer baseline.

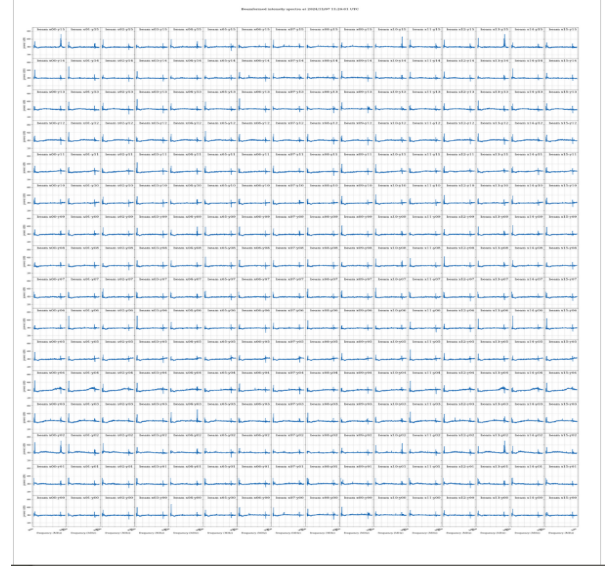


Figure 1. Spectra of 256 beamformed beams. X axis is 400 to 800MHz.

BURSTT is a two-dimensional beamforming array. We implemented the first beamformer in a RFSoc FPGA (ZCU216) while the second beamforming was performed in the Intel Xeon server. The RFSoc unit accommodates 16 analog-to-digital (ADC) channel inputs, sampling data at 1600 MHz at a bandwidth of 800MHz. Sixteen signal inputs are processed independently using a Polyphase filter bank (PFB) and fast Fourier transform (FFT) [6]. After frequency domain data is obtained, a 16×16 weight factor matrix was applied to perform the initial round of beamforming. This process generates 16 beams, after which we combined the data for all 16 channels, then packetized the data and sent them to the server through a 100 Gbps Ethernet (hereafter 100GbE) connection for a second round of beamforming. We elaborated the second beamforming code in the server by using an Intel 4th-generation Xeon CPU: Intel(R) Xeon(R) Platinum 8458P.

Advanced Matrix Extension 512 (AMX512) [7] command is used to perform data manipulation and beamforming. One server processed four ZCU216 boards, and one ZCU216 accommodated 16 antenna inputs. A 256-beams snapshot as shown in Fig. 1, was taken from the main site.

II. SENSITIVITY

The dipole antenna we employed, has the advantage of a wider field of view. Conversely, its disadvantage is lower sensitivity. To enhance sensitivity, we are planning to implement more antennas at the main sites. Currently, we sample the 0 to 800MHz band; However, we only use the data from 400 to 800MHz, which has a bandwidth of 400MHz. Only half of the bandwidth is used. To make the FPGA more efficient, we are designing a system to combine two antenna inputs into one ADC channel.

To accommodate two antenna inputs into one ADC channel, the signals from the even-numbered antennas must be filtered out 0 to 400MHz band out of the original 0 to 800MHz bandwidth to retain 400-800 MHz band. Consequently, only 400 to 800MHz bandwidth remains. The signal from odd-numbered antennas must first be manipulated as if they were even-numbered antenna. After isolating 0-400 MHz signal only 400 to 800 MHz band remains and we down-converted this 400 MHz band to the 0 to 400MHz range. Finally, a signal combiner combines the 0-400 MHz signal from the odd-numbered antennas and 400MHz to 800MHz signal from even-numbered antennas.

Due to the characteristic of microwave filter, it is challenging to achieve extremely sharp filtering device. Therefore, there exist guard bands, which are unused frequency band, as illustrated in Fig. 2. As the guard bands are unignorable, we have to increase the sampling rate, thus cover those unused guard bands.

Refer to the data sheet of the FPGA chip on the board ZU49DR-2, [8] its maximum block RAM (Random Access Memory) and FIFO (First-In, First-Out) switching frequency is 516MHz, thus we made two attempts, 460MHz and 500MHz clocking rate in the FPGA, those are equivalent to 1920 and 2000MHz sampling rates, and 920 and 1000 MHz bandwidths respectively

We summarized the timing summary reports of different designs obtained after compilation in the Vivado design suite are illustrated in Table 1. The Worst Negative slack (WNS) is a key metric in digital design timing analysis, mostly used in FPGA and ASIC design to represent worst timing violation in a circuit. If WNS value less than zero indicates the design does not fully meet the timing requirement.

In our design with 500MHz clock frequency, we observed higher timing score (WNS and TNS) as expected. At 460MHz, the timing score slightly exceeded the timing constraint. However, since the timing score was not severe, we made an attempt to implement the 460MHz bitstream to the FPGA board. We then tested the spectrum capture and the 100GbE packet transmission, both of which functioned correctly.

TABLE I. COMPARISON OF TIMING SCORES

	Timing Violation (ns)		
	400MHz	460MHz	500MHz
Worst Negative Slack	0	-0.227	-0.462
Total Negative Slack	0	-232.550	-1942.034

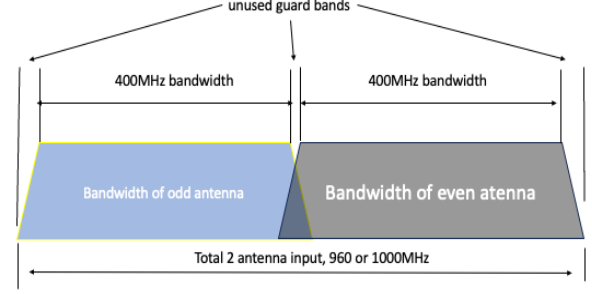


Figure 2. Two antennas signal into one ADC channel. Odd antenna occupies the lower half of the band, and even antenna occupies the upper half of the band. Unused guard bands will be discarded only two of the 400MHz band reserved.

III. SUMMARY

The main site and one outrigger station of BURSTT are ready for FRBs detection. We have tested the system by post processing the observed data and detected the Crab giant pulses and B0329+54 pulse. We have demonstrated the possibility to accommodate two antennas input into one ADC channel with bandwidth of 920MHz. With installation of more antennas resulting more signal collection, BURSTT will be more sensitive to detect the FRBs.

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