

A High Sensitivity Transceiver Design Using Step Recovery Diodes for GPR Applications

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Abstract— In this study, a new GPR transceiver having sub-nanosecond pulser and sample-and-hold structure designed with step recovery diodes is described. The amplitude and pulse width of the transmit part in the transceiver has 40V peak-to-peak and 800 picoseconds, respectively. In the receiver part of the transceiver, a high sensitivity receiver unit is obtained by integrating the pulse shaping structure in the pulser to the sample-and-hold circuit. This efficiency has been carried out by a critical selection of RF balun and bridge diode structure. In this way, the sampling circuit having peak-to-peak amplitude 3V and pulse duration of 200 picoseconds has been produced. Thanks to the high amplitude of the sampling circuit, the sensitivity of the GPR system is increased. The sampling signal and noise performance of the designed transceiver has been illustrated with measurement data.

I. INTRODUCTION

Ground Penetrating Radar (GPR) systems can be designed with both frequency and time domain technology for many years [1]. The impulse technology has frequently been preferred to the GPR systems since it has fast response and obtains high resolution. To detect buried objects with high resolution, the system needs narrow pulse width. Generally, the pulser circuits can be generated using avalanche transistors or step recovery diodes (SRDs) [2]. Avalanche transistors can produce very fast response and high pulse voltage pulses and are widely used for GPR applications. However, the disadvantage of the avalanche transistor is that it requires a high voltage source. For this reason, both power consumption and physical dimension of the circuit increases [3]. On the other hand, the pulser circuits designed by SRD do not need a high voltage source and it provides low power consumption. [4]. Received signal convert digitalize via high sample rate analog to digital converters (ADC) for digital signal processing unit. The received signal can reproduce from sampled data using a low-speed ADC by the help of sample-and-hold circuits. This solution is cheaper than high speed ADC solutions [5]. There are various sampling diode architecture circuits in the literature. The most important of these are two diode and four diode sampling architectures. Comparing these two sampling architectures, the four-diode system has a lower frequency band than the two-diode system. However, a four-diode bridge reduces the crosstalk between the input signal and the sampled signal [6].

In this paper, a new transceiver architecture design using SMMD-810 SRD diode is described [7]. Using this SRD, a pulse generator with high amplitude has been designed in the transmitter part of the system. The same SRD pulser structure has been applied in the receiver block to obtain a low noise and high sensitivity sample-and-hold circuit. Finally, the sampled

signal and noise performance of the proposed system is presented.

II. TRANSCEIVER DESIGN

It has been used in the SRD pulser circuit in the transmitter part of the proposed design as referred [8]. The square wave trigger can apply to the circuit in the range of 100 kHz-1 MHz and the circuit operates with drawing current in the range of 40-50 mA from 12 V supply. The pulse repetition frequency of the square wave to input of the transmitter is 250 kHz with 0-5V. Thus, it has produced a Gaussian pulse having 45V peak-to-peak amplitude and 790 picosecond pulse width at the output of the transmitter. The circuit block diagram, and measurement results are shown as in Fig. 1.

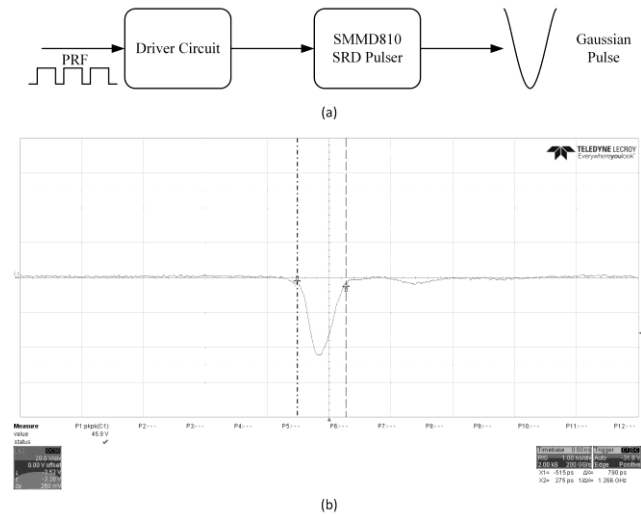


Figure 1. (a) The block diagram of pulser circuit and (b) output of the pulser.

In the receiver part of the system, the same pulser block has been used to obtain sampling pulses. In the time domain, the pulser of the receiver is symmetrized with RF balun [9].

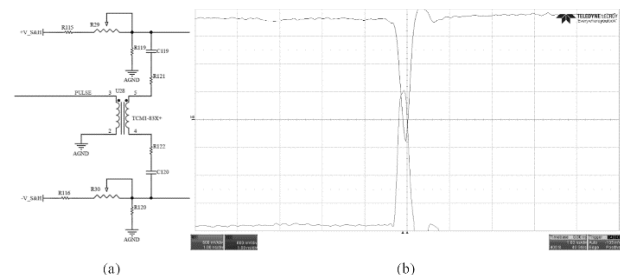


Figure 2. (a) Sampling pulses divider schematic and (b) sampling pulses.

In this way, sampling pulses having approximately the same positive and negative amplitude are obtained. Because of high bandwidth (10-8000 MHz), low phase unbalance (4-8 degree), and low attenuation (1.3 dB), TCM1-83X+ has been used as a balun [10]. Schematic diagram of the sampling pulse generator is shown in Figure 2(a). The resulting sampling pulse measurement is also shown in Figure 2(b). In the measurement in Figure 2(b), each frame in the vertical is 0.6V and each frame in the horizontal is 1 ns. When the result is examined, since the forward voltage value of the diode used is 0.23V, a sampling pulse of approximately 200 ps width with 2.23V offset and 0.67V amplitude has been obtained. Thanks to the symmetrical structure of the same pulse, received signal in the GPR system can be easily sampled up to $\pm 2.23V$. It has been explained in the introduction section that there are different methods applied in mixer design. A four-diode mixer design has been used because it provides good isolation between the input signal and the sampled signal. The block diagram of the designed sample-hold system is shown in Figure 3. The impedance of the signal at the output of the bridge has been first increased with the buffer op-amp. Then, switching noises have been filtered and analog gain has been added to the signal and transferred to the ADC. The designed PCB is shown in Figure 4.

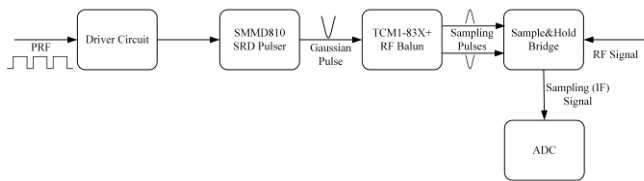


Figure 3. The block diagram of sample-hold system.

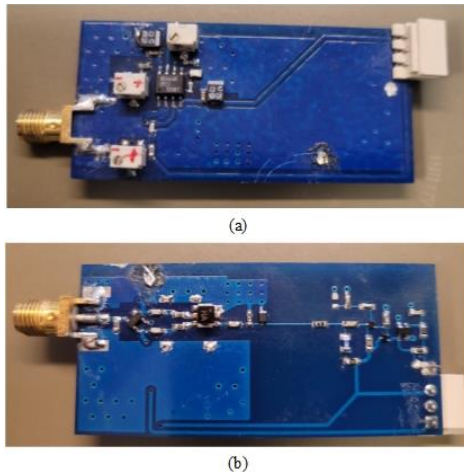


Figure 4. (a) Top view of PCB and (b) bottom view of PCB.

To evaluate the sampling performance, the signal to noise ratio (SNR) of the signal transferred to the ADC has been measured. The SNR measurement is shown in Figure 5. While the received signal has an amplitude of 600 mV and a noise level of approximately 20 mV, the sampled signal multiplied by the gain has an amplitude of 1700 mV and a noise level of approximately 50 mV. According to these results, the SNR value of the incoming signal has been increased after the sampling process.

CONCLUSION

In this paper, it is explained how to design a high sensitivity GPR transceiver. In the transmitter structures, sub-nanosecond pulse generator block diagram and measurement result are given. Then, it is explained how the same pulse generator has been integrated to the received structure. The implementation results of the sampling structure have been explained. Finally, the SNR measurement of sampled signal has been presented.

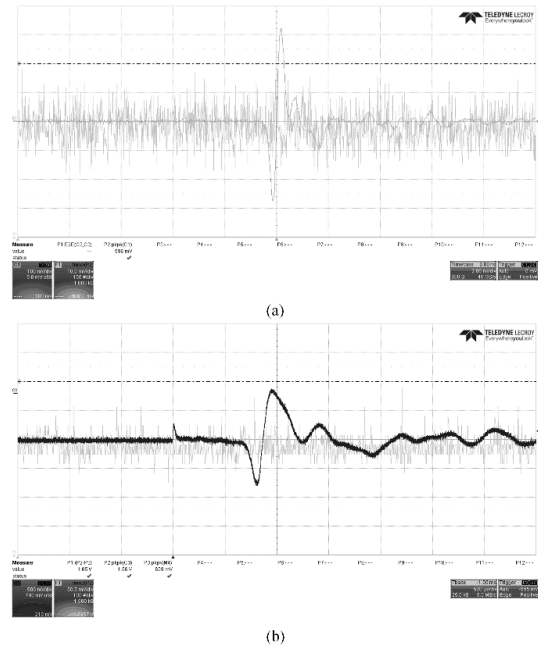


Figure 5. (a) Received signal and (b) sampled signal noise measurement.

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