

Wide-Band Component Less Bias Tee Compatible with Standard PCB Process

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Abstract—This paper presents the design and implementation of a bias tee component on a single-layer PCB using a lumped-element-free approach. The DC block features a modified finger structure loaded with ceramic powder, along with an E-shaped slot to improve bandwidth. A parametric study was performed to optimize the number of fingers in the DC block. Experimental results confirmed a bandwidth of 8:1, with the lower frequency extending down to 1 GHz.

I. INTRODUCTION

The need for wideband components is continuously increasing, particularly for 6G, as the demand for high data rates and flexible communication systems grows. The bias tee network separates the DC biasing source from the microwave input-output signals in active circuits such as amplifiers, oscillators, mixers, or switches. This three-terminal network enables the input and output ports to route microwave signals to the integrated active device within the structure with a DC supply applied to the third port [1]. Capacitors are commonly used to separate DC from RF loads and sources, while inductors are utilized to reduce RF leakage at the third port.

This application requires high-quality capacitors to effectively reduce losses. SMD capacitors are frequently employed, but their performance restricts the potential voltage used. Distributed elements can also be utilized for simpler component designs or high-power applications, such as power amplifiers. Distributed capacitors have been extensively designed using many different approaches. Some are very complex, such as the fully integrated bias tee with a capacitor [2] or with metal insulator metal capacitor (MIM) [3]. These designs are useful for demanding applications with a compact size, but require a high complexity of fabrication. Two-layer printed circuit boards (PCBs) or more are necessary for designs that are less complex. In order to achieve a low-complexity and low-cost design, a distributed capacitor can be achieved using conductive fingers on a single layer.

At higher frequencies, the parasitic effects of distributed capacitors become more significant, and finger-introduced self-resonance of the inductor is a major challenge. The self-resonant frequency will deteriorate the band by introducing losses. In [4], a bias tee component less ultra broad band was realized in a single layer. A bias tee with a large bandwidth was achieved, but it requires an advanced fabrication process due to the minimum gap needed being less than $20\ \mu\text{m}$. This high resolution is not obtainable from a classical PCB fabrication process and it is usually not suitable for low cost fabrication. The standard process components that are available for PCBs are restricted to a minimum of $75\ \mu\text{m}$.

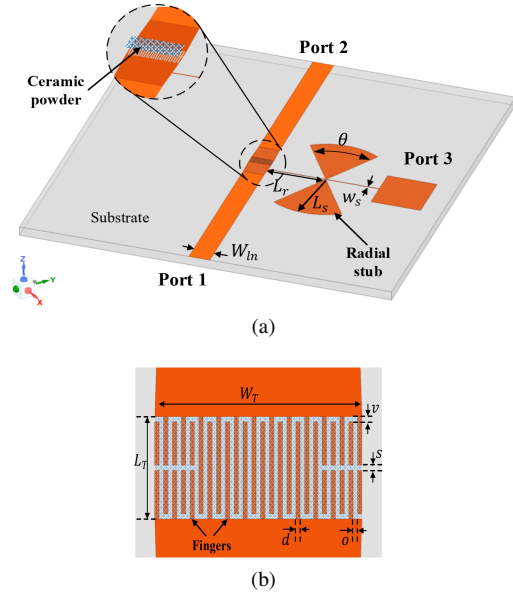


Fig. 1: (a) 3D view of the proposed design ($W_{in} = 3.35\ \text{mm}$, $L_s, L_r = 10.3\ \text{mm}$, $\theta = 32^\circ$, $W_s = 75\ \mu\text{m}$). (b) Interdigital capacitor loaded with $Nb = 5$ ($d, o, v, s, = 75\ \mu\text{m}$, $W_t = 3.58\ \text{mm}$, $L_T = 1.5\ \text{mm}$).

In this paper, a new design of distributed capacitors compatible with commercial low-cost fabrication process is proposed and applied for a bias tee. Section II explains the design theory by showing the equivalent model. The fabrication and experimental results are presented in section III

II. DESIGN STRATEGY

For the design, a well-known inter digital capacitor is used [5]. This type of capacitors are widely utilized in RF and microwave circuits because of their compact size, high quality factor, and seamless integration with PCB manufacturing techniques. These capacitors consist of alternating conductive fingers, which create capacitance through fringing electric fields between them. However, these structures are not exclusively capacitive; they also exhibit inherent inductive characteristics due to the current flowing along the conductive fingers. At resonance, the inductive reactance counteracts the capacitive reactance, resulting in a condition of resonance. This phenomenon creates a transmission zero at a specific frequency at which signal propagation is significantly attenuated and impose limitations on the usable bandwidth of the capacitor. As a result, designers must carefully optimize the

physical dimensions, spacing, and layout of the interdigital capacitor to minimize the impact of unwanted resonances while maintaining the desired capacitance characteristics.

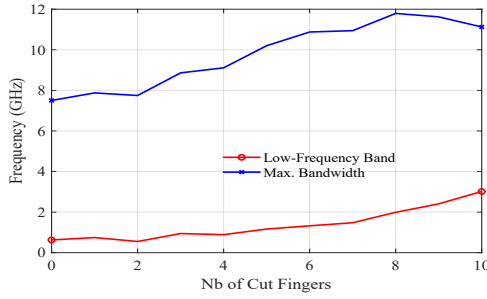


Fig. 2: Variation of maximum -3dB bandwidth and low-frequency band versus to the number of cut fingers.

The conventional technique described in [4] increases resonance by reducing the gap, which increases manufacturing requirements. In this study, self-resonance is mitigated by incorporating slots to reduce inductance. However, this approach also influences the value of the capacitor, leading to an increase in the minimum frequency. Consequently, an optimization of the trade-off is required to improve the maximum available bandwidth. The number of cut fingers will move the self resonance frequency and then, increase or decrease the bandwidth. To decrease the lower frequency, the interdigital capacitance is artificially increased by loading the gap with alumina powder.

The initial capacitor with a large number of fingers (12) is used. Thus, a parameter study was performed to evaluate the optimum configuration in order to maximize the bandwidth. Two slots were placed in the middle of the inter-digital capacitor, cutting the fingers in two parts. The firsts fingers with a slot was on the both side, and then, when the length of the slot was increased, more fingers were cut up to the middle finger. The study was realized with different width of the slots. Figure 2 show the variation of the maximum bandwidth and the low frequency band function to the number of fingers. The max bandwidth increase with the Nb of fingers to reach a maximum of 12 GHz as well as the low frequency band. The minimum frequency increase since the capacitor value decrease as well the Nb of cut finger.

III. EXPERIMENTAL RESULTS

Figure 3 depicts the prototypes fabricated in a PCB single layer using RO4350B as substrate ($\epsilon=3.5$, $\tan \delta = 0.0037$) with 1.6 mm of thickness and Nb of cut finger = 2. A gap of 75 μm is used, which is compatible with any standard PCB process. The results show good agreement between measured and simulated data from 1 to 8 GHz. The density of the powder leads to the entrapment of air, which reduces the effective permittivity, thereby causing performance degradation below 1 GHz. However, this achieved ratio of 8:1 is unparalleled in the literature. (5:1 in [4])

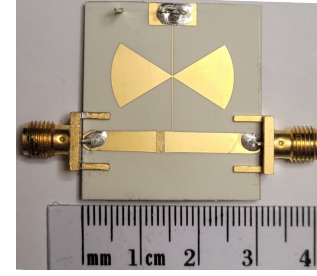


Fig. 3: Photograph of fabricated prototype.

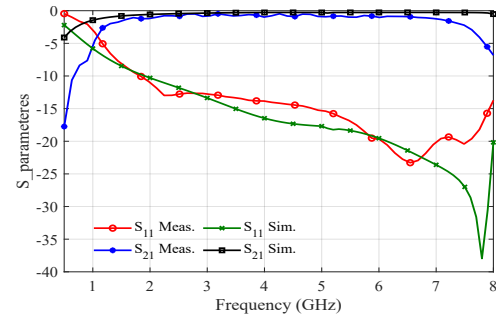


Fig. 4: Simulated and measured S-parameters of the proposed Bias TEE.

IV. CONCLUSION

This paper presented a modified interdigital capacitor with double radial stubs to design a bias tee with improved fractional bandwidth and minimum frequency. To reduce the low-frequency band, different methods were explored, and a solution using slots and loaded capacitor was proposed. A study of the parasitic elements in the interdigital capacitor was carried out, which helped in designing a bias tee with both large bandwidth and simpler fabrication requirements. A prototype was built to confirm the simulation results, and the measurements showed a fractional bandwidth of 150%. During measurements, problems were detected with the RF isolation in the DC port. Further work is required to reduce the frequency dependence of the isolation.

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