A Four-Element Digital Array Receiver at 2.4 GHz Using a Single Frequency-Multiplexed ADC

Arjuna Madanayake[1], Najath Akram*[1], Elias Alwan[1], Satheesh Venkatakrishnan[1], John Volakis[1], Soumyajit Mandal[2], and Leo Belostotski[3]

[1] Florida International University, Miami, Florida, USA
[2] Case Western Reserve University, Cleveland, Ohio, USA
[3] The University of Calgary, Alberta, Canada

Digital phased- and time-array receivers are critical components of wireless communication links and for radio-astronomy infrastructure. As system bandwidths continue to increase, wideband data conversion at each antenna receiver becomes increasingly challenging for large arrays. Emerging 5G communication systems, for example, may require fully-digital transceivers capable of several independent radio frequency (RF) beams that may necessitate individual analog to digital converters (ADCs) for each antenna/receiver pair. Since higher order modulation, such as orthogonal frequency division multiplexing (OFDM), requires high signal to noise ratio (SNR) for low bit-error rates, antenna array receivers must correspondingly have at least 4-5 bits of precision per ADC to guarantee an acceptable dynamic range. Notably, multi-bit ADC topologies (flash converters, voltage-to-time-to-digital converters) are associated with high power consumption. Therefore, large number of these high-precision ADCs is not always practical.

Recently, a method known as "on-site coding receiver (OSCR)" has been successful in reducing the number of ADC channels for a given antenna array. OSCR employs a series of analog multipliers fed by unique binary coded waveforms (-1 and 1) at each receiver output. The binary coded waveforms are typically Walsh-Hadamard (WH) codes, and the coded signals are summed, and sampled using a single high-speed over-sampling ADC. Once digitized, the original channels can be recovered with minimal to no signal degradation using cross-correlation based digital signal processing (DSP). This OSCR approach has resulted in significant hardware (ADC and DSP) reduction by almost 87%.

In this paper, we expand OSCR to use frequency division multiplexing instead of orthogonal WH coding. Input channels will be frequency translated using a bank of phase- and frequency-locked oscillators at known frequency off-sets. Unlike OSCR, the frequency-division multiplex (FDM) approach does not require quasi-static conditions for the receiver signals to be satisfied. The sampled signal is then recovered using a linear finite impulse response (FIR) filterbank followed by a series of digital down-converters. The oscillators will be synchronized using a stable low-jitter reference clock (100 MHz) via a bank of integer-N frequency synthesizers. At the digital back-end, we explore the application of maximally-decimated uniform-discrete-Fourier-transform polyphase and quadrature mirror filterbanks, and other DSP systems, with digital quadrature hybrids. A prototype to combine 4 channels, each at 250 MHz bandwidth per channel, interfaced to a Xilinx Virtex-6 FPGA. This paper will discuss trade-offs between dynamic range, effective number of bits, ADC power consumption per channel and per bit, and system complexity for a given level of performance.