SDR-Based Wireless Time Alignment for Coherent Distributed Beamforming

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Coherent distributed systems offer a cost effective and efficient alternative to traditional platform-centric radar models for performing collaborative tasks. Significant gains can be achieved in transmit power and spatial diversity compared to single platform systems, since the transmit gain scales as the number of platforms squared. These low cost platforms can in the future be used for surface imaging, soil moisture mapping and other remote sensing applications (J.A. Nanzer *et. al.*, IEEE Transactions on Microwave Theory and Techniques (MTT-S), May 2017, vol. 65, no. 5, pg. 1662-1672). Most device clocks are crystal based and are subject to drift because of various physical effects. Consequently clock alignment along with relative frequency and initial phase locking are essential for a fully functional coherent distributed system. Depending upon how the system achieves its phase and time synchronization, distributed arrays can be broadly categorized as Open-loop or Closed-loop. Our approach is the Open-loop type which does not involve a feedback from the destination for phase and clock correction.

In this work we utilize the FPGA available on the Ettus X310 Software Defined Radios to demonstrate the timestamp-free synchronization protocol (D.R. Brown III and A.G. Klein, Information Sciences and Systems (CISS), Mar 2013) for time transfer at radio frequencies. The timestamp-free protocol accounts for propagation delay and is performed at the physical layer unlike other conventional protocols which rely on exchange of timestamps. Out of the two channels on the Ettus X310s one channel is used for exchanging a sync pulse for internode coordination and the other for coherent pulse transmission. The internal computation engine (CE) clock on the FPGA serves as reference for any clock calculations. A predetermined number of CE ticks equal one user defined tick (UD). A sync pulse being sent out from the slave node gets time mirrored across one UD tick of the master node and retransmitted. Upon reception of the sync pulse at the slave node, the UD clock offset is calculated and corrected for. In other work (M.W.S. Overdick *et. al.*, IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), Mar 2017, pg. 1193-1197) the processing is done in the host computer, controlling the radio, leading to indeterministic delay with the signal traveling back and forth between the host and radio. Our approach processes the signal on the FPGA making it more suitable for a physcial layer realization. Measurements are taken to demonstrate the signal gain of the coherent distributed system.