Voltage Doubler Rectenna Design with Surface Waves Suppression

M. Fairouz[(1)]
(1) The Higher Institute of Telecommunication and Navigation, PAAET, Kuwait

A voltage doubler rectenna using circularly polarized microstrip patch antenna with reduced surface waves is proposed. A rectenna operating at 5.8 GHz has been designed and simulated in Advanced Design System (ADS). Tow zero bias Schottky diodes with high detection sensitivity are used as rectifying device as well as voltage doubler. In order to minimize surface waves, two microstrip circular patch antennas with shorting pins are used.

In (J. Zbitou, M. Latrach and S. Toutain, Microwave Theory and Techniques 55, PP 147-152, 2006) the reported RF-DC conversion efficiency rectenna using zero bias diode is reached to 68%. In this work, the maximum RF-DC conversion efficiency for a voltage doubler rectenna (two zero bias diode) has been achieved to 75% for input power of 11 dBm. The corresponding output DC voltage is 3.2V. On the other hand, the efficiency for a single zero bias diode is reached to 70% with output DC voltage of 1.6V.

The patches are modified by inserting four shorting pins to suppress surface waves, and therefore, minimize the mutual coupling between the array elements (M.Fairouz and M. Saed, PIERC 55, PP 179-186, 2014). This modification will result in improved overall array performance by having higher gain, better radiation pattern, and better beam scanning capability (avoiding scan blindness). The shorting pins will also eliminate the need for an RF chock present in traditional rectenna designs.

The block diagram of proposed rectenna is illustrated on Fig.1. The substrate used is RT/Duroid 6010 with a dielectric constant $\varepsilon_r = 10.2$ and thickness of 1.27mm. In this design, the outputs of the two antenna array elements are combined using a 50Ω Wilkinson power divider. The Wilkinson power divider is chosen in this design because of its high isolation between two ports. A microstrip bandstop filter is designed to pass 5.8GHz from the antenna to the voltage doubler diode and block the second harmonic 11.6GHz. The filter uses λ/4 (at 11.6 GHz) open-circuited shunt stubs to block the second harmonic.

The two diodes used in the proposed rectenna design are a zero bias Schottly detector diode (HSMS-2852). It has high sensitivity, up to 25mV/uW at 5.8GHz. The diode model parameters are: series resistance R_s = 25Ω, zero-bias junction capacitance C_{j0} = 0.18pF, breakdown voltage V_B = 3.8V, and maximum forward voltage V_F= 150mV. Two capacitors (C1 and C2) are included in the design as a part of voltage doubler circuit. The input impedance of a voltage doubler at 5.8 GHz is $Z_d = 6.6 - j17.1\ \Omega$. A matching circuit using single, open-circuited shunt stub was used to match Z_d to =50Ω. A low pass filter capacitor C2 (2.2nF) and the load resistance (2.6KΩ) were optimized in ADS in order to reach the highest RF-DC conversion efficiency.

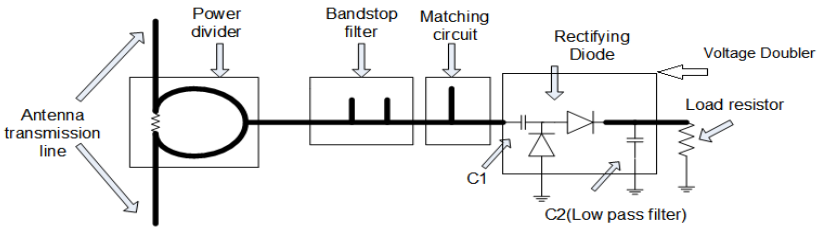

Figure 1. The block diagram of proposed rectenna design.