GaN-on-Si with CMOS Integration for Advanced, Low Cost Phased Arrays

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Phased array systems have benefitted from the industrial push towards higher levels of electronic system integration. Until recently, phased arrays were constructed with relatively physically deep "slats" to house array electronics behind the radiating elements. Such packaging was necessary to contain bulky and costly electronics modules, RF and power cabling, and thermal management components within the confines of a phased array unit cell width (e.g. typically $\lambda_0/2$, or 50 mm at 3 GHz). Great cost reductions in phased array systems have been achieved in the past several years with the adoption of planar, panel-based phased arrays. In contrast to slats, these panels leverage modern multi-layer printed circuit board fabrication and automated surface mount assembly technologies to reduce material (packaging and cables) and assembly costs. Panel-based arrays face challenges at higher frequencies, however, where lattice dimensions and the available component area becomes smaller. Especially at 10 GHz and above, reducing the number of integrated circuits and passive devices behind each element is required to realize the array. Such a parts count reduction also lowers the overall system cost.

This talk describes a wafer-scale 3D heterogeneously integrated circuit technology combining GaN-on-Si and Si-CMOS devices (Fig. 1), and its application to advanced phased array systems. In this technology wide-bandgap GaN high electron mobility transistors (HEMT) are used for power amplifiers, low noise amplifiers, switches, and other circuits requiring high power handling or high voltage swing while CMOS is used for dense digital, mixed signal, and low-power analog circuits. The combination of technologies enables a transmit/receive (T/R) module system-on-chip (SoC) with high performance RF, analog, and digital functionality. Such a single IC T/R solution enables low cost microwave and millimeter-wave phased arrays with advanced features such as power amplifier envelope tracking and digital signal processing.

An overview of the technology development work will be provided including details on material growth, device fabrication, and circuit design and modeling. We will also present the latest MMIC results and our progress towards a phased array implementation using this technology.

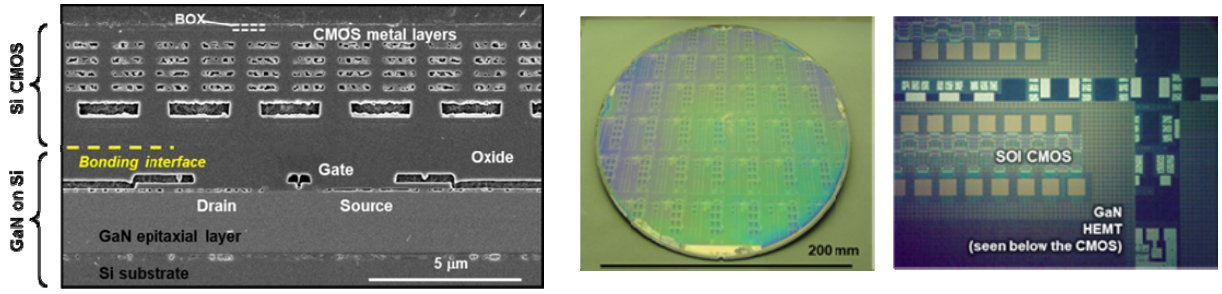

Figure 1. (Left) Cross section of a bonded GaN-on-Si and CMOS wafer, (center) a fabricated 200-mm-diameter 3D integrated wafer, and (right) a top view of a 3D circuit showing both CMOS and GaN circuits.

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