Gain Enhancement of mm-wave On-chip Antenna through Functional Packaging

Haoran Zhang and Atif Shamim
Division of Computer, Electrical, and Mathematical Science and Engineering (CEMSE)
King Abdullah University of Science and Technology (KAUST)
Thuwal, 23955-6900, Saudi Arabia
Haroan.zhang@kaust.edu.sa; Atif.shamim@kaust.edu.sa

With the proliferation of wireless devices, 5G and beyond concepts, there is increasing interest to achieve high levels of integration and higher data rates at lower costs. At mm-wave, the wavelength is small enough to realize the antenna-on-chip (AoC), which is the ultimate solution for compactness and lower cost. However, the main drawback AoC is the low resistivity (10 Ω-cm) Si substrate used in standard CMOS technology, which causes most of the RF power to be absorbed by Si rather than being radiated by the on-chip antenna. Moreover, due to the high relative permittivity (11.9) and relatively large electrical thickness of the Si, high order surface waves modes get excited, which further degrade the antenna radiation performance (H. M. Cheema and A. Shamim, IEEE Microw. Mag., 14, 79-91, 2013).

To overcome the challenges mentioned above, several solutions have been proposed. One approach is to alter the silicon substrate structure (through micromachining to reduce the thickness) or properties (through proton implantation to enhance the resistivity) (H. Chu et al., IEEE Trans. Antenna Propag., 60, 4582-4588, 2012; K. T. Chen et al, IEEE Microw. Wireless Compon. Lett., 13, 487-489, 2003). In some cases, Si substrate is isolated from the antenna by using an Artificial Magnetic Conductor (AMC) surface in between (M. Nafe et al., IEEE Antenna Wireless Propag. Lett., 16, 2844-2847, 2017). Some designs use superstrates to enhance the performance (J. M. Edwards et al., IEEE Trans. Antennas Propag., 60, 5010-5020, 2012). On the other hand, every chip needs to be packaged for protection from environment and this chip package can be utilized smartly to enhance antenna's performance.

In this work, a CPW-fed monopole on-chip antenna at 71 GHz, along with the corresponding driving circuit, is designed and fabricated in a standard 0.18 μm CMOS process. In order to overcome the low gain and efficiency of the on-chip antenna, we have first utilized an AMC structure within the chip environment. Further gain and efficiency enhancement are achieved by smartly designing the package into a combination of a superstrate and Fresnel lens. This way the package is not a mere protection cover, but it is functional and provides gain enhancement. The overall combination of optimized AMC surface, superstrate layer and lens package can provide a gain enhancement of around 17 dBs. The concept of functional packaging can be very important for futuristic wireless devices in the era of 5G and beyond.