

A Repeater Optimization Methodology for Global Multi-Walled Carbon Nanotube Interconnects

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Abstract—In this paper, the optimal repeater number and size are analyzed for multi-walled carbon nanotube interconnects by using the particle swarm optimization (PSO) algorithm. Genetic algorithm (GA) is also used to verify the corresponding results. Further, the neural network (NN) is trained to facilitate the EDA process. It is found that the computational time can be dramatically reduced with the implementation of NN.

Keywords—Carbon nanotube, interconnect, neural network, particle swarm optimization, repeater insertion.

I. INTRODUCTION

With the continuous development of CMOS technologies, the gate delay and the local wire delay decrease rapidly. However, as the length increases with the scaling down of feature size, the time delay of global interconnect increases and has become an urgent problem to be solved in current very large scale integration (VLSI) [1].

As an alternative conductor, multi-walled carbon nanotube (MWCNT) has attracted a lot of research interests in the past decades. MWCNT has many extraordinary properties, including long mean free path (MFP) and high ampacity. Moreover, the repeater insertion technique is always employed to improve the interconnect performance in the design of high-performance ICs. It is natural to insert repeaters in a long MWCNT interconnects. Unfortunately, it is found that a repeater design methodology that targets minimum time delay may lead to overestimation of the number of repeaters, thereby resulting in excessive power dissipation [2].

In this paper, a model that considering the influence of metal-CNT contact resistance has been developed. In the model, the input variables consist of interconnect width, length, and contact resistance at a specific technology node, while the outputs include the optimal repeater size and number. Inputs and outputs form a database to train the machine learning algorithm to create mappings between the geometrical parameters and optimal repeater design. The rest of this paper is organized as follows. In Section II, the electrical model of MWCNT interconnect is presented. The simulated results are

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analyzed in Section III. Some conclusions are finally drawn in Section IV.

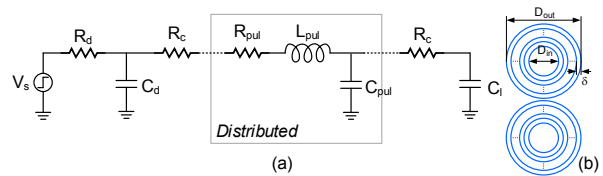


Fig. 1. (a) Equivalent circuit model of the driver-interconnect-load (DIL) system. (b) Cross-sectional views of MWCNT interconnect.

TABLE I. GLOBAL INTERCONNECT PARAMETERS

Technology Node		14 nm	7 nm
Interconnect width W		≥ 21.5 nm	≥ 10.5 nm
Wire aspect ratio (H/W)		2.34	2.4
ILD aspect ratio (T/W)		1.5	1.5
Effective dielectric constant ϵ_r		2.08	1.65
Minimum-sized gate	Driver resistance R_{d0}	30.3 k Ω	69.7 k Ω
	Driver capacitance C_{d0}	0.22 fF	0.13 fF
	Load capacitance C_{l0}	0.15 fF	0.06 fF

II. EQUIVALENT CIRCUIT MODEL

Fig. 1(a) depicts the equivalent circuit model of a driver-interconnect-load system. R_d , C_d , and C_l represent the driver resistance, driver capacitance and load capacitance, while R_{pul} , L_{pul} , C_{pul} are per-unit-length (p.u.l.) resistance, inductance, and capacitance of the MWCNT interconnect, respectively. R_c denotes the contact resistance. Fig. 1(b) shows the cross-sectional view of an MWCNT interconnect, with its geometrical parameters summarized in Table I.

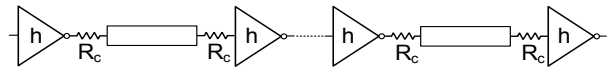


Fig. 2. Repeater insertion in a long global MWCNT interconnect.

Generally, the repeaters are uniformly inserted in a long global interconnect, as shown in Fig. 2. The interconnect is divided into k segments, and each segment has a length of L/k . The driver resistance, driver capacitance, and load capacitance of a repeater are R_{d0}/h , hC_{d0} , and hC_{l0} , where h is the size of the repeater. The 50% time delay of one

segment can be calculated by

$$T_s = (1.48\xi + e^{-2.9\xi^{1.35}}) \sqrt{\frac{L_{pul}L}{k} \left(\frac{C_{pul}L}{k} + hC_{l0} \right)} \quad (1)$$

where $\xi = [R_T + C_T + 0.5 + R_T C_T (1 + C_{d0}/C_{l0})] / \sqrt{1 + C_T \cdot (R_t/2) \cdot \sqrt{C_{pul}/L_{pul}}}$, $C_T = hC_{l0}/C_t$, $R_T = R_{d0}/(hR_t)$, $C_t = C_{pul}L/k$, and $R_t = R_{pul}L/k + 2R_c$. The total time delay of the global MWCNT interconnect is $T_{total} = kT_s$. The energy dissipation consumed by one segment is approximated by $P_s = [C_{pul}L/k + h(C_{d0} + C_{l0})]V_{dd}^2$, and the total power dissipation is $P_{total} = kP_s$ [3]. Here, the figure of merit (FoM) of the global MWCNT interconnect is given as $F = P_{total} \cdot T_{total}$.

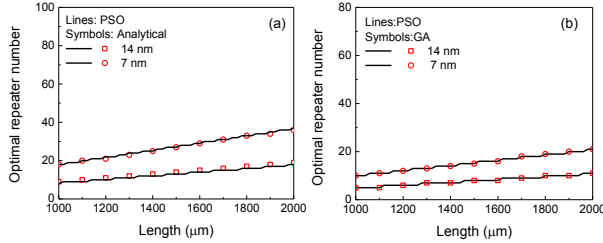


Fig. 3. Optimal number of the repeaters in global MWCNT interconnects at the 14 nm and 7 nm technology nodes in the (a) delay and (b) power delay product (PDP)-optimal repeater designs.

III. RESULTS AND DISCUSSION

By utilizing the PSO algorithm, the optimal repeater size and optimal number of repeaters in a global MWCNT interconnect can be obtained numerically. To validate the PSO algorithm, a global MWCNT interconnect is taken as example, and the minimum time delay is assumed as the optimization goal. Fig. 3(a) shows the optimal number of repeaters in an MWCNT interconnect at the 14 nm and 7 nm technology nodes. The solid lines are obtained by the PSO algorithm, while the symbols are captured analytically. It can be seen that these results agree well with each other. Moreover, it is evident that the optimal number of repeaters increases with the scaling down of interconnect dimensions. Further, Fig. 3(b) shows the optimal repeater design targeting the minimum power delay product (PDP). In the figure, the solid lines and symbols are obtained by the PSO algorithm and genetic algorithm (GA), respectively, and these results agree well with each other.

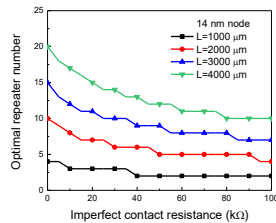


Fig. 4. Optimal number of repeaters in SWCNT bundle interconnects with different lengths at the 14 nm technology nodes.

The influence of imperfect contact resistance between the MWCNT interconnect and metal electrode on the repeater design is studied. As shown in Fig. 4, the optimal number of

repeaters decreases rapidly with the increasing contact resistance.

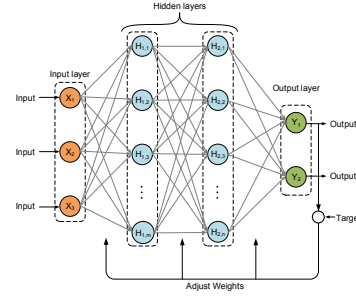


Fig. 5. Schematic of the back propagation neural network.

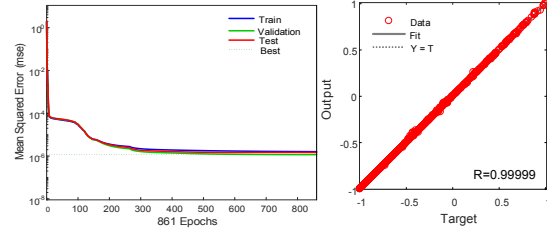


Fig. 6. (a) Squared error versus epoch curves and (b) NN output versus target regression curves for MWCNT interconnects at the 14 nm technology node in the PDP-optimal repeater designs.

As the optimal repeater size and optimal number of repeaters in the MWCNT interconnect have been calculated by using the PSO algorithm, these results can be employed to train the neural network (NN), as shown in Fig. 5. Fig. 6(a) shows the number of iterations of the NN to achieve convergence. Here, the target of mean square error (MSE) is set as 10^{-8} . The recursive process of the learning algorithm ends as the error cannot be reduced anymore. Further, the comparison between the outputs of the NNs and the desired targets are shown in Fig.6(b). good fit is indicated as the solid and dashed lines completely overlap with each other. The optimal repeater size and optimal number of repeaters can be obtained easily by using the trained NN. In particular, it costs approximately 55 hours to capture these optimal values by using the PSO algorithm, while the computation time can be reduced to 4.43 s for the same datasets by using the trained NN.

IV. CONCLUSION

In this study, the optimal repeater design was analyzed for global MWCNT interconnects. Both the time delay and power dissipation have been considered and addressed appropriately. The feasibility of the machine-learning neural network (NN) in the optimal repeater designs was discussed. It was demonstrated that the trained NNs can predict the optimal number of repeaters and optimal repeater size rapidly and accurately.

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