A Full-Duplex Radio Using a CMOS Non-Magnetic Circulator Achieving $+95\,\text{dB}$ Overall SIC

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***Abstract*—Full-duplex (FD) wireless is an emerging wireless communication paradigm where the transmitter and the receiver operate simultaneously at the same frequency. One major challenge in realizing FD wireless is the interference of the TX signal saturating the receiver, commonly referred to self-interference (SI). Traditionally, self-interference cancellation (SIC) is achieved in the antenna, RF/analog, and digital domains. In the antenna domain, SIC can be achieved using a pair of separate TX and RX antennas, or using a single antenna shared by the TX and RX through a magnetic circulator, which is usually bulky, expensive, and not integrable with CMOS. Recent advances, however, have shown the feasibility of realizing high-performance non-reciprocal circulators in CMOS based on spatio-temporal modulation. In this work, we demonstrate a high power handling FD radio using a USRP SDR which employs SIC (i) at the antenna interface using a watt-level power-handling CMOS integrated, magnetic-free circulator, (ii) in the RF domain using a compact RF canceler, and (iii) in the digital domain. Our prototyped FD radio achieves $+95\,\text{dB}$ overall SIC at $+15\,\text{dBm}$ TX power level. We analyze the effects of the circulator TX-RX non-linearity on the total achievable SIC.**

***Index Terms*—Circulator, CMOS, full-duplex, non-reciprocity, self-interference cancellation.**

I. Introduction

Today's wireless systems are half-duplex (HD), where the transmission and reception of radio signals are separated in either different time slots (e.g., time-division duplexing, TDD) or different frequency bands (e.g., frequency division duplexing, FDD). Full-duplex (FD) wireless is an emerging technology which allows simultaneous transmission and reception at the same frequency, and has the potential to improve the spectral efficiency at the physical (PHY) layer and to provide many other benefits at the higher layers [1]–[3]. Therefore, FD can possibly be applied to many applications including PHY layer security, relaying and forwarding, and network synchronization and localization. Simultaneous transmit and receive capability is also critical to commercial and DoD radar systems.

The fundamental challenge associated with FD wireless is the tremendous amount of self-interference (SI) leaking from the transmitter (TX) into the receiver (RX), which needs to be canceled to successfully receive the desired signal. This is usually achieved through SI suppression at the antenna interface (using a pair of antennas or a single antenna through a circulator) and the self-interference cancellation (SIC) in the RF/analog and digital domains. Recent research has shown the feasibility of integrating circulators in CMOS through spatio-temporal modulation [4] and most recently, architectural advances have enabled these CMOS time-modulated circulators to achieve watt-level transmitter power handling and wideband and tunable isolation [5]. In this work, we present an FD radio using this highly linear CMOS circulator [5], which achieves high TX power handling of upto $+16\,\text{dBm}$ (limited by overall SIC) and $+95\,\text{dB}$ overall SIC across the antenna, RF, and digital domains. We also analyze the effects of the circulator TX-RX non-linearity on the achievable SIC.

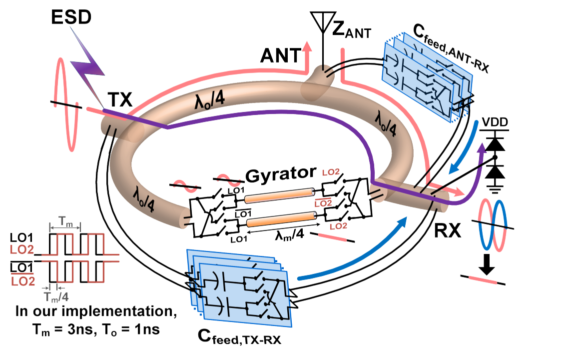

Fig. 1. High power handing circulator with inductor-free antenna balancing.

II. A Full-Duplex Radio Prototype Using the CMOS Magnetless Circulator

We implement an FD radio prototype, which consists of an antenna, the integrated magnet-free CMOS circulator with inductor-free loss-free antenna balancing [5], a conventional frequency-flat amplitude- and phase-based RF SI canceller [6], and a USRP2 software-define radio (SDR).

A. Architecture and Implementation Details

Fig. 1 shows the concept diagram of the highly linear RF CMOS integrable circulator [5] used in realizing this FD radio. The circulator is implemented using the concept of switched transmission lines [7], [8], and it exploits the feature of lowering of the modulation frequency to improve the linearity and power handling. The switches are modulated at 333MHz for 1GHz operation, and such a low modulation frequency enables the usage of the thick-oxide devices in 180nm SOI CMOS technology to boost power handling. This circulator achieves 10–100× better linearity/power handling compared to our prior work [4]. In addition, this circulator employs an antenna balancing scheme which uses tunable feed-capacitor circuits between TX and RX, and ANT and RX ports, to produce orthogonal cancellation currents to cancel the TX leakage at the RX port of the circulator.

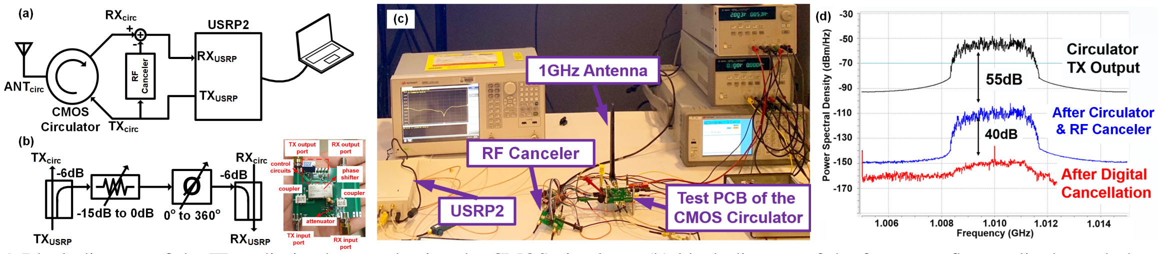

Fig. 2. (a) Block diagram of the FD radio implemented using the CMOS circulator, (b) block diagram of the frequency-flat amplitude- and phase-based RF canceler, (c) measurement setup of the FD radio with the CMOS circulator, (d) measured spectra with a $+15$ dBm, 10 MSa/s QPSK signal provided at the TX of the circulator in the prototyped FD radio.

The circulator has measured insertion losses of $2.1/2.9$ dB in the TX-ANT/ANT-RX paths, and a measured ANT-RX noise figure of 3.1 dB. Using the tunable switched capacitor banks, $>$40 dB TX-RX isolation is achieved across the entire 1.85 ANT VSWR variation and beyond. The measured in-band TX-ANT and ANT-RX IIP3s are $+50.03$ dBm and $+36.9$ dBm, respectively. The TX-ANT input $P_{1\text{dB}}$ is $>$ $+30.66$ dBm (limited by the measurement setup), at which point the compression is only 0.66 dB, while the ANT-RX input $P_{1\text{dB}}$ is $+21.01$ dBm.

Fig. 2(a) shows the block diagram of the prototyped FD radio. The 0.8–1.3 GHz RF canceller (see Fig. 2(b)) taps a reference signal at the USRP TX output and performs SIC at the USRP RX input. The residual SI after the circulator isolation and RF SIC is further suppressed in the digital domain, where the digital SI canceller is implemented using non-linear tapped delay lines.

B. Effect of Circulator Non-Linearity on the SIC

Imperfect SIC may result in lower FD rate gains due to the residual SI above the RX noise floor [9]. At high TX power levels, the circulator TX-RX non-linearity can limit the amount of SIC that can be achieved by the FD radio. Unlike the non-linearity from a power amplifier (PA), the IM3 terms from circulator cannot be canceled in the RF/analog domain as the portion of PA output coupled into the RF canceler does not contain the information of the non-linear terms created by the circulator. However, these non-linear terms can be canceled in the digital domain using the digital SIC. The TX-RX IIP3 of this circulator when tuned to achieve the maximum isolation of $+50$ dB is $+24$ dBm. The total SI power introduced by the 3$^{\text{rd}}$-order non-linearity at the RX port of the circulator is given by $P_{\text{rx,IM3}} = (P_{\text{tx}} - 50) - 2 \times (24 - P_{\text{tx}}) = (3P_{\text{tx}} - 98)$ dBm. With a USRP noise floor of $P_{\text{nf}} = -90$ dBm for 10 MHz signal bandwidth (includes environmental noise), a $+16$ dBm TX signal results in an non-linear SI power of -90 dBm after digital SIC (i.e., $P_{\text{rx,IM3}} - 40$ dB digital SIC with $P_{\text{tx}} = +16$ dBm), which is equal to USRP receiver noise floor. Therefore, for TX power levels greater than $+16$ dBm, residual SI is increased due to the non-linear components along with the fundamental components, which will lead to lower SIC and lower FD rate gains at the same link SNR value. In other words, better exploiting the watt-level power handling at the circulator TX port will require either improving circulator TX-RX IIP3 or better nonlinear digital cancellation algorithms.

C. SIC Measurement of the FD Node

A $+15$ dBm, 10 MSa/s QPSK signal is provided at the TX port of the circulator, and the SI spectra after the circulator isolation and RF cancellation, and after the digital cancellation are shown in Fig. 2(c). The residual SI power $P^{\text{res}}_{\text{SI,linear}} + P^{\text{res}}_{\text{SI,non-linear}} \approx -80$ dBm and is dominated by $P^{\text{res}}_{\text{SI,linear}}$. Hence, this FD radio achieves $+95$ dB overall SIC across the antenna, RF, and digital domains. We remark that an extra analog canceller as reported in [3], [4], [10] can potentially achieve further improved SIC, and the overall SIC of the FD radio will be limited by the circulator TX-RX non-linearity.

III. Conclusion

We presented an FD radio prototype with a CMOS integrable circulator which performs SIC in the antenna, RF, and digital domains. The implemented FD radio achieves $+95$ dB overall SIC, where $+55$ dB is achieved by the circulator and the RF canceller, and $+40$ dB is achieved by the digital SIC. We also presented an analytical analysis on how the circulator TX-RX non-linearity limits the overall SIC. We remark that improving the TX-RX non-linearity of the CMOS integrable circulator is a subject of future research.

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