Clock Synchronization Challenges for On-Site Coding Digital Beamformer

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Typical radio frequency (RF) digital beamformers can be highly complex. In addition to a suitable antenna array, they require numerous receiver chains, demodulators, data converter arrays, and digital signal processors. To recover and reconstruct the received signal, synchronization is required since the analog-to-digital converters (ADCs), digital-to-analog converters (DACs), field programmable gate arrays (FPGAs), and local oscillators (LO) are all clocked at different frequencies. An additional issue is caused by the requirement of serial interfaces to the transmit/receive blocks. This implies that data and clock blocks need be embedded/de-embedded by a digital processor or FPGAs.

As can be realized, clock/time synchronization is essential to achieving and maintain coordination among independent local clocks within each component in a transmitter/receiver in a beamforming system. Such synchronization is challenging as it may lead to undesired clock jitter. It is therefore necessary to include circuits for jitter attenuation to avoid system degradation. Further, poor sampling clocks may lead to high phase noise, hence giving rise to degradation of the signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

With the above in mind, we propose a clock synchronization topology for a multi-channel on-site coding receiver (OSCR). To achieve synchronization, devices in this system must 1) have direct access to timing signals from a common source, or 2) must synchronize their individual clocks to a common time base. But in the context of on-site coding, N-coded channels are combined into a single ADC. This approach reduces synchronization errors by a factor of N, as compared to a conventional digital beamformer. At the conference, we will present the advantages of the on-site coding architecture in terms of reducing synchronization errors in realizing digital beamformers. We will also demonstrate a clock synchronization implementation for an 8-channel on-site coding digital beamformer using an FPGA and off the shelf components. Specifically, we will show the generation of different signals and their synchronization across the components. We will also discuss other possible synchronization techniques for a distributed RF system.