94 GHz VCO Using Negative Capacitance Technique

Yo-Sheng Lin, Kai-Siang Lan, Yun-Wen Lin, and Ming-Yuan Chuang

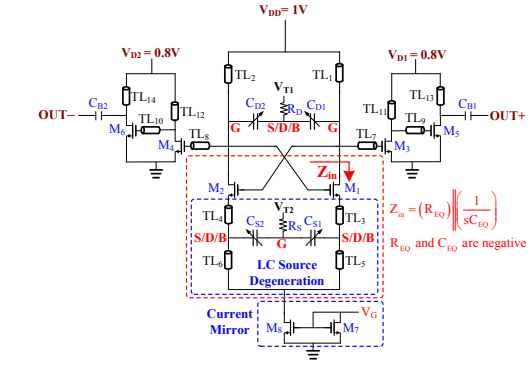
Department of Electrical Engineering, National Chi Nan University, Puli, Taiwan, R.O.C.
Tel: 886-4-92912198, Fax: 886-4-92917810, Email: stephenlin@ncnu.edu.tw

***Abstract*—A 94 GHz voltage-controlled oscillator (VCO) using both LC-source-degeneration-based (LCSD-based) negative capacitance technique and series-peaking gain enhancement technique is demonstrated in a 90 nm CMOS process. The LCSD-based negative capacitance is made by adding two tunable LC tanks, which use NMOSFET varactors as the needed capacitors, to the source terminals of the cross-coupled transistor pair of the VCO. Compared with the traditional cross-coupled transistor pair, the proposed one significantly decreases the tunable equivalent parallel capacitance (C_{EQ}) to zero and even a negative value. This in turn results in the increase of both the operation frequency and the tuning range of the VCO. The VCO draws 8.3 mA current from a 1 V power supply, i.e. it only consumes 8.3 mW. The VCO achieves a tuning range of 91~96 GHz. In addition, the VCO achieves an excellent low phase-noise of –98.3 dBc/Hz at 1 MHz offset from 95.16 GHz. The corresponding FOM is –188.5 dBc/Hz, one of the best results ever reported for a V- or W-band CMOS VCO. The circuit occupies a small chip area of 0.75×0.42 mm^2, i.e. 0.315 mm^2, excluding the test pads.**

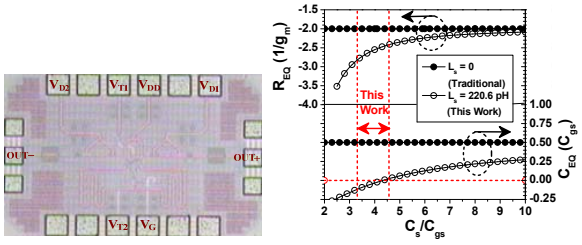
Keywords—CMOS; VCO; negative capacitance; W-band

I. Introduction

Some of the negative-resistance-cell-based oscillator architectures include ring oscillator, relaxation oscillator, and LC oscillator. Nowadays, in high-speed transceiver applications, LC VCO is the most popular one mainly because high-Q integrated inductors are available. The traditional negative-resistance cell constitutes a crossed-coupled transistor pair. The corresponding input impedance is equal to a negative resistance of $-2/g_m$ in parallel with a capacitance of $C_{gs}/2$, where g_m and C_{gs} are the transconductance and the gate-source capacitance of transistor, respectively [1]. For high frequency LC VCO, the ratio of $C_{gs}/2$ to the equivalent capacitance of the LC tank is high, which in turn degrades the operation-frequency and the tuning-range. Recently, researchers have made some proposals to reduce the parasitic capacitance of the traditional negative-resistance cell. For instance, the capacitive source-degeneration negative-resistance cell is proposed in [2]; however, only simulation data are available and the operation-frequency of 5.3 GHz is not high enough. In [3]-[4], the LC source-degeneration negative-resistance cell is proposed to further reduce the power dissipation, and the push-push technique is used to achieve dual-band operation. In this work, we propose a 94 GHz VCO using both the LCSD-based negative capacitance and the series-peaking gain enhancement techniques. The tunable equivalent parallel capacitance (C_{EQ}) of the cross-coupled transistor pair can be reduced to zero and even a negative value. This is the way to enhance the operation frequency and the tuning range of the VCO.



(a)



(b) (b)

Fig. 1 (a) Schematic diagram, and (b) chip micrograph of the proposed 94 GHz VCO. (c) Calculated R_{EQ} and C_{EQ} versus C_s/C_{gs} characteristics in the condition of $\omega/\omega_T = 0.549$ based on (3)-(4).

II. Circuit Design

Fig. 1(a) shows the schematic of the proposed VCO. The current mirror constitutes transistors M_7 and M_8 can provide stable bias current to the VCO core. Fig. 1(b) shows the chip micrograph of the proposed VCO. The chip area is only 0.75×0.42 mm^2, i.e. 0.315 mm^2, excluding the test pads. The equivalent L_s and C_s of the proposed LCSD-based cross-coupled transistor pair can be expressed as follows.

$$L_s \approx TL_3 + TL_5 \tag{1}$$

$$C_s \approx \frac{C_{s1}}{1+TL_3/TL_5} \tag{2}$$

After calculation, equivalent resistance R_{EQ} and equivalent capacitance C_{EQ} can be derived as follows:

$$R_{EQ} = \frac{-2}{g_m} \cdot \frac{[1+(\frac{\omega}{\omega_T})^2(1+\frac{C_s}{C_{gs}})^2 - 2(\frac{\omega_1}{\omega_T})^2(1+\frac{C_s}{C_{gs}})] + \frac{\omega_1^4}{\omega^2\omega_T^2}}{[(\frac{\omega}{\omega_T})^2\frac{C_s}{C_{gs}}(2+\frac{C_s}{C_{gs}}) - 2(\frac{\omega_1}{\omega_T})^2(1+\frac{C_s}{C_{gs}})] + \frac{\omega_1^4}{\omega^2\omega_T^2}}$$

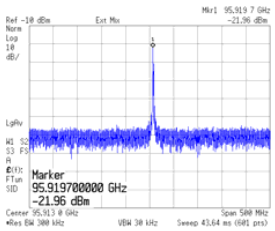
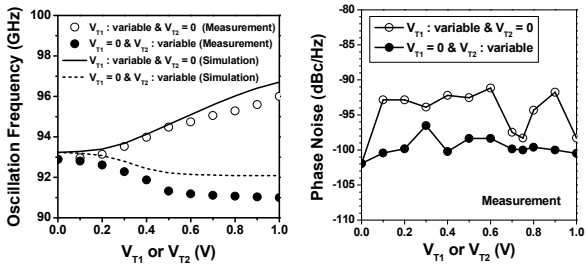


Fig. 2 Measured single-ended output spectrum.



(a) (b)

Fig. 3 (a) Measured and simulated oscillation frequency, and (b) measured phase noise versus V_{T1} or V_{T2} characteristics of the VCO.

Table I A summary of the 94 GHz CMOS VCO, and recently reported state-of-the art VCOs with similar operation frequency.

	V_{DD} (V)	P_{DC} (mW)	ω_0 (GHz)	PN (dBc/Hz)	FOM (dBc/Hz)	CMOS Process (nm)
This Work	1	8.3	93.6	–98.3	–188.5	90
[1]	1.2	54	105	–92.8	–175.9	65
[2]	1.2	15	97.2	–80	–168	90
[3]	1.2	2.6	70	–78.7	–171.5	110
[4]	1	10.4	59.3	–81.7	–167	65

$$\approx \frac{-2}{g_m} \qquad (\text{if } C_s \text{ and } L_s \to 0) \tag{3}$$

$$C_{EQ} = \frac{C_s}{2} \cdot \frac{\frac{\omega_2^2}{\omega^2} + \frac{\omega_1^2}{\omega_T^2}\frac{\omega_2^2}{\omega^2} + \frac{\omega^2}{\omega_T^2}(1+\frac{C_s}{C_{gs}}) - \frac{\omega_1^2}{\omega_T^2} - \frac{\omega_2^2}{\omega_T^2}(1+\frac{C_s}{C_{gs}}) - 1}{\frac{\omega_1^4}{\omega^2\omega_T^2} + \frac{\omega^2}{\omega_T^2}(1+\frac{C_s}{C_{gs}})^2 - 2\frac{\omega_1^2}{\omega_T^2}(1+\frac{C_s}{C_{gs}}) + 1}$$

$$\approx \frac{C_{gs}}{2} \qquad (\text{if } C_s \text{ and } L_s \to 0) \tag{4}$$

in which $\omega_T = g_m/C_{gs}$ is the current-gain cut-off frequency of the cross-coupled transistors M_1 and M_2, $\omega_1 = 1/\sqrt{L_s C_{gs}}$, and $\omega_2 = 1/\sqrt{L_s C_s}$.

Fig. 1(c) shows the calculated R_{EQ} and C_{EQ} versus C_s/C_{gs} characteristics in the condition of $f/f_t = 0.549$. As can be seen, C_{EQ} decreases with the decrease of C_s/C_{gs}. The expense is an increase of the magnitude of the negative resistance R_{EQ}. That is, there is a trade-off between C_{EQ} reduction and the possibility of oscillation start-up. To minimize C_{EQ} for high frequency operation and to make sure oscillation start-up, selection of a C_s/C_{gs} value below than 8 is reasonable. In this work, corresponding to V_{T2} tuning range of 0~1 V, C_s/C_{gs} ranges 3.3~4.6. The corresponding R_{EQ} and C_{EQ} are $-2.41/g_m$ ~ $-2.83/g_m$ and 0 ~ $-0.118C_{gs}$, respectively. Since C_{EQ} is equal to zero or a negative capacitance (for reducing the overall capacitance of the VCO), both the operation frequency and the tuning range of the VCO can be effectively enhanced.

III. Results and Discussions

The VCO core and buffer amplifiers draw bias currents from 1 V and 0.8 V power supplies, respectively. The VCO only consumes 8.3 mW. Fig. 2 shows the measured oscillation frequency and single-ended output power of the VCO at V_{T1} = 1 V and V_{T2} =0 V. The measured oscillation frequency is 95.92 GHz, and the corresponding single-ended output power (i.e., OUT+ or OUT– only, the other port connected to 50 Ω terminal) is –14 dBm (if the measured cable loss of 8 dBm is considered).

Fig. 3(a) shows the measured and simulated oscillation frequency versus V_{T1} or V_{T2} characteristics of the VCO. The VCO achieves a tuning range of 91~96 GHz, close to that of the simulated one (92.1~96.7 GHz). In addition, the VCO achieves single-ended output power of –8.2~ –14.1 dBm (not shown here). Fig. 3(b) shows the measured phase noise (at 1 MHz offset from the center frequency) versus V_{T1} or V_{T2} characteristics of the VCO. The VCO achieves phase noise of –91.2~ –101.9 dBc/Hz. Table I is a summary of the implemented 94 GHz CMOS VCO, and recently reported state-of-the-art VCO with similar operation frequency. Compared with the measured results in other pieces of work, our VCO exhibits low power consumption, and one of the best phase noises and FOMs. These results indicate that our proposed VCO architecture is suitable for both V- and W-band transceiver front-end applications.

IV. Conclusion

In this work, we propose a CMOS VCO architecture using LCSD-based negative capacitance technique and the series-peaking gain enhancement technique. The VCO achieves a tuning range of 91~96 GHz, and a low phase-noise of –98.3 dBc/Hz at 1-MHz offset from 95.16 GHz. The corresponding FOM is –188.5 dBc/Hz, one of the best results ever reported for a W-band CMOS VCO. These results indicate that the VCO is suitable for V- and W-band communication systems.

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