95/190 GHz Push-Push VCO in 90 nm CMOS

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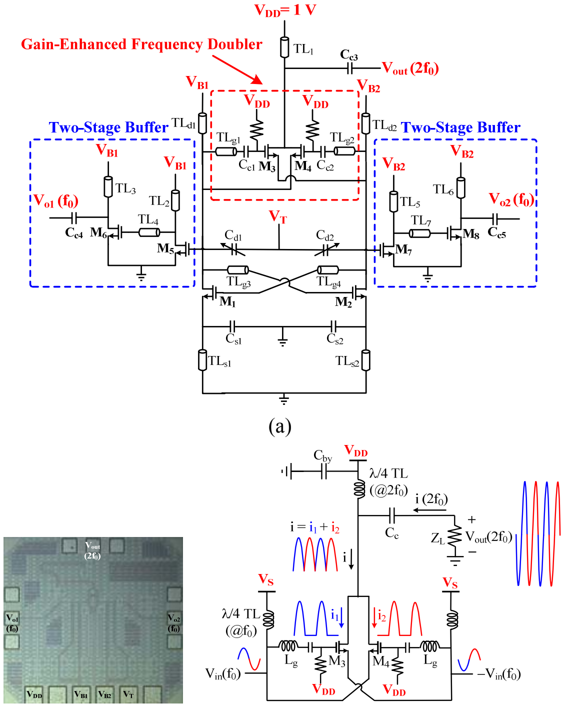
***Abstract*—A 95/190 GHz voltage-controlled oscillator (VCO) using gain-enhanced frequency doubler is demonstrated in 90 nm CMOS. Compared with the traditional push-push architecture, the proposed one can significantly increase the second-harmonic output signal due to the inductive series-peaking gain-enhancement of the full-wave-rectifier-based frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the transistors of the VCO. The VCO consumes 12 mW. At the fundamental port, the VCO achieves a tuning range of 92.6~95 GHz, and a low phase-noise of –88.2 dBc/Hz at 1 MHz offset from the center frequency. The corresponding FOM is –177 dBc/Hz. At the push-push port, the VCO achieves a tuning range of 185.2~190 GHz, and a low phase-noise of –82.5 dBc/Hz at 1 MHz offset from the center frequency. The corresponding FOM is –177.3 dBc/Hz. To the authors' knowledge, the phase noise and FOM performances of the VCO are one of the best results ever reported for a W-band or G-band CMOS VCO.**

Keywords—CMOS; push-push; VCO; W-band; G-bands

I. INTRODUCTION

Normally, the fundamental oscillation frequency of an LC VCO is limited by the unity power gain frequency f_{max} of the cross-coupled transistors. To implement a VCO with oscillation frequency higher than f_{max}, push-push VCO, which uses the second-harmonic frequency tone based on nonlinearity of the cross-coupled transistors, has been proposed in [1]. However, the nonlinearity-based push-push VCO suffers from two issues. One is high power dissipation because high bias current is normally needed to generate sufficient second-order nonlinearity of the transistors. The other is that it is usually required to drive a high-impedance following stage, which makes it hard to be compactly implemented. In [2], a fundamental-signal-based push-push VCO using g_m-boosted full-wave rectification technique is proposed to enhance the second-harmonic output signal. Compared with the traditional full-wave rectification technique, the improvement in the second-harmonic output signal is smaller than 100%. In the present work, in order to achieve low power, low phase-noise, high output power (much higher than 100%), and high-frequency operation at the same time, we propose a 95/190 GHz push-push VCO using both the gain-enhancement frequency doubler and current reuse techniques. The second-harmonic output signal can be significantly enhanced due to the inductive series-peaking gain-enhancement of frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the cross-coupled transistors of the VCO.



(a)

(b) (c)

Fig. 1 (a) Circuit diagram, and (b) chip photo of the 95/190 GHz CMOS VCO. (c) The proposed frequency doubler.

II. CIRCUIT DESIGN

The push-push VCO with a full-wave-rectifier-based frequency doubler was designed by a 90 nm CMOS process. Fig. 1(a) shows the schematic of the proposed push-push VCO. Compared with the traditional push-push architecture, the proposed one can significantly increase the second-harmonic output signal due to the inductive series-peaking gain-enhancement of the frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the cross-coupled transistors of the VCO. Fig. 1(b) shows the chip micrograph of the push-push VCO. The chip area is only 0.58×0.61 mm^2, i.e. 0.35 mm^2, excluding the test pads. Fig. 2 illustrates the operation principle of the frequency doubler using the inductive series-peaking gain-enhancement technique. Transistors M_3/M_4 are biased at class-B, so each one contributes half-wave current rectification to realize the full-wave current rectification.

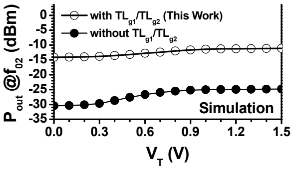
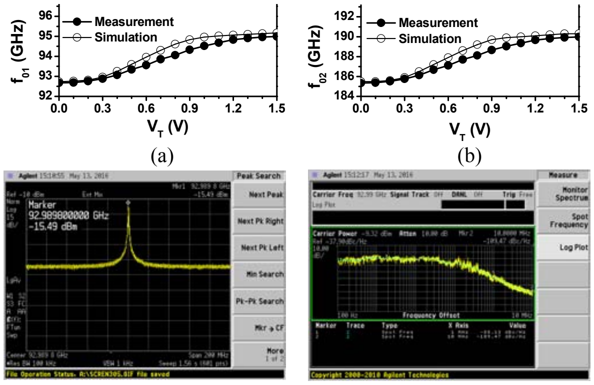


Fig. 3 Simulated single-ended output power at f_{02} versus V_T characteristics of the VCO



(a) (b)

(c) (d)

Fig. 4 Measured and simulated (a) f_{01} and (b) f_{02}, and measured (c) single-ended output spectrum, and (d) phase noise at f_{01} of the VCO.

Fig. 3 shows the simulated single-ended output power versus tuning voltage (V_T) characteristics at the push-push port of the VCO both with and without the series-peaking gain-enhanced inductors TL_{g1}/TL_{g2}. The VCO in our case achieves the better single-ended output power of −11.2~ −14.1 dB at the push-push port. In comparison, in the case without the peaking inductors TL_{g1}/TL_{g2}, the single-ended output power is only −24.8~ −30.4 dBm at the push-push port.

III. CIRCUIT DESIGN

The VCO core and buffer amplifiers draw bias currents from 1 V and 0.5 V power supply (Agilent 6624A), respectively. The VCO only consumes 12 mW. Fig. 4(a) shows the measured and simulated oscillation frequency versus V_T characteristics at the fundamental port of the VCO. The VCO achieves a tuning range of 92.6~95 GHz, close to that of the simulated one (92.7~95.2 GHz). Fig. 4(b) shows the measured and simulated second-harmonic frequency f_{02} versus V_T characteristics of the VCO. The VCO achieves a tuning range of 185.2~190 GHz, close to that of the simulated one (185.4~ 190.4 GHz). Fig. 4(c) shows the measured oscillation frequency and single-ended output power of the VCO at the fundamental port (at V_T = 0.35 V). The measured oscillation frequency is 93 GHz, and the corresponding single-ended output power (i.e., $V_{o1}(f_0)$ or $V_{o2}(f_0)$ only, the other port connected to a 50 Ω terminal) is −8.5 dBm (if the measured cable loss of 7 dBm is taken into account). Fig. 4(d) shows the measured phase noise of the VCO at the fundamental port at V_T = 0.35 V. The VCO achieves an excellent low phase-noise of −88.1 dBc/Hz at 1 MHz offset (from the center frequency of 93 GHz).

Table I Summary of the implemented 95/190 GHz CMOS VCO, and recently reported state-of-the-art MMW CMOS VCOs.

	P_{DC} (mW)	Freq. (GHz)	PN @1 MHz Offset (dBc/Hz)	FOM (dBc/Hz)	Process (nm)
This Work	12	95	88.2	177	90
		190	82.5	177.3	
[2]	14.6	80.7	84.2	166.9	90
[3]	54	105	92.8	175.9	65
[4]	15	97.2	80	168	90
[5]	2.6	70	78.7	171.5	110
[6]	10.4	59.3	81.7	167	65

A widely-used figure-of-merit (FOM) for a VCO is defined as follows.

$$\mathrm{FOM} = \mathrm{L}(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\ \mathrm{mW}}\right) \qquad (1)$$

where L(Δf) is the measured phase noise at Δf frequency offset from the carrier frequency f_o in dBc/Hz, and P_{DC} is the dc power dissipation in mW. Table I is a summary of the implemented 95/190 GHz CMOS VCO, and recently reported state-of-the-art millimeter-wave VCO. Compared with the measured results in other pieces of work, our VCO exhibits low power consumption and phase noise, and one of the best FOMs. These results indicate that our proposed VCO architecture is suitable for both W-band and G-band transceiver front-end applications.

IV. CONCLUSION

In this work, we propose a push-push VCO with a full-wave-rectifier-based frequency doubler, in which the inductive series-peaking gain-enhancement technique is used to improve the second-harmonic output signal. Since the bias current of the frequency doubler is reused by the VCO core, low power dissipation is available. At both the fundamental and push-push ports, the VCO achieves excellent tuning range, phase noise and FOM performances, one of the best results ever reported for a W-band or G-band VCO. These excellent results lead to the conclusion that the proposed VCO is suitable for both W-band and G-band communication systems.

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