Phase Characterization of an 8-Channel On-site Coding Receiver for Digital Beamforming

Satheesh Bojja Venkatakrishnan*, Abe A. Akhiyat, Elias A. Alwan,
Waleed Khalil, and John L. Volakis
ElectroScience Laboratory, Electrical and Computer Engineering Dept.
The Ohio State University, Columbus, Ohio, 43212.
e-mail: bojjavenkatakrishnan.1@osu.edu

Ultra-wideband (UWB) systems combined with the advances in digital signal processing and data handling have drastically reduced the complexity of cognitive and software defined radios. Therefore, techniques such as monopulsing, multiple beams, among others, can be implemented for phased arrays and Multiple Input Multiple Output (MIMO) systems. A major drawback in MIMO systems is hardware redundancy after each antenna element. This implies challenges in high power, cost, and area requirements. To this end, a number of hardware reduction techniques at handling the RF front-end have been proposed. They include spatial multiplexing (SM), time-division multiplexing (TDM), and frequency division multiplexing (FDM). But these techniques are based on time slots or bandwidth sharing making them inadequate in terms of resource utilization.

A way to overcome the aforementioned challenges is to employ newly introduced on-site coding receiver (OSCR) architecture. This receiver relies on code division multiplexing (CDM) introduced right after the antennas, to significantly reduce the intense hardware requirement for digital beamforming [Alwan et. al., Springer, 2013]. Specifically, the down-converted baseband signal from each antenna is coded with a unique orthogonal code at the analog front-end prior to combining all signal paths into a single Analog to Digital Converter (ADC). More specifically, a single ADC digitizes the combined signals replacing the requirement for using many ADCs one per antenna element. The digitized signals are then decorrelated at the digital back-end using algorithms in FPGA. Code decorrelation followed by matched filtering, is carried out within the FPGA to recover the individual array element signals and perform digital beamforming.

The proposed beamformer was already tested and verified for 2 signal paths. In this paper, we conduct a system analysis for up to 8 signal paths per ADC. The goal is to assess phase and decoding errors caused by the hardware and complex post-processing associated with these systems. Specifically, as the number of channel increases, co-channel cross-talk becomes significant. Highly orthogonal codes with minimum cross-correlation are then required to minimize interference. Our main objective is to faithfully estimate angle of arrival of incoming signals and perform beamforming at the digital back-end. To do so, it is necessary to ensure proper LNA calibration, filtering, blocker rejection, and a large enough ADC dynamic range for sufficient phase/angle recovery. More details on the implementation and analysis of the proposed 8-channel communication system will be presented in the conference.