Wideband SiGe Low Noise Cryogenic Amplifier for the SKA

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One of the major instruments within the Square Kilometre Array (SKA) project is the SKA1_Mid which consists of 254 15m reflector telescopes to be located in South Africa. As currently planned there are 5 cryogenic receivers on each of the telescopes covering the frequency range of 0.35 to 13.8 GHz. As a cost reduction and frequency range extension strategy, Wideband Single-Pixel Feeds are being investigated as a means of achieving 1.6 to 24 GHz frequency coverage with just two receivers, band A for 1.6 to 5.2 GHz, and band B for 4 to 24 GHz.
Caltech has been contracted by the Beijing Astrophysical Observatory in China to design an LNA for SKA band A. The design and first test results for this cryogenic amplifier are the focus of this paper.

Caltech has experience with the design, fabrication, and testing of both HEMT MMIC amplifiers such as the CITCRYO1-12 covering 1 to 12 GHz and SiGe discrete transistor amplifiers such as the CITLF4 covering 0.5 to 4 GHz. For the 1.6 to 5.2 GHz SKA application, the SiGe discrete transistor approach was selected for the following reasons: 1) the noise is likely to be lower, in the range of 2K, 2) it is easier to obtain good input match at low microwave frequencies with bipolar transistors, 3) the discrete SiGe transistors are easier to obtain than wideband cryogenic MMICs, 4) the SiGe bipolar transistor amplifiers are extremely repeatable and this facilitates the manufacture of the hundreds of amplifiers that will be required, and 5) a single DC voltage of approximately 2V can power the amplifier.

Design of the amplifier commenced in late 2014 with goals in the 1.6 to 5.2 GHz range of 2K noise, >30 dB gain flat to within +/-1 dB, input and output return loss < -10 and -15 dB respectively. In addition, for stability the input to output isolation, S21 + S12, must be < -10 dB for all frequencies. The initial design utilizes a STMicroelectronics chip transistor as the first stage and NXP commercial, packaged transistors for the 2^{nd} and 3^{rd} stages. Current simulation results indicate that these specs are achievable using this design. The transistor models used in these simulations were developed at Caltech by Bardin and Russell as part of their Ph.D. thesis work. Much effort has been spent modeling the parasitics of the resistors, capacitors, and inductors used in the amplifier.

Fabrication and testing of the prototype amplifier is expected by the end of March, 2015 and test results will be reported at the URSI conference. Further work will include design improvements, design for manufacture, and reliability testing.