Dynamic Crosstalk Analysis of CMOS Driven *RLC* Interconnects using FDTD Method

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The scaling of on-chip interconnect dimensions and high operating frequencies produce transient crosstalk between coupled interconnect lines. Because of this reason, the estimation of propagation delay and crosstalk noise becomes a critical issue. In this paper, an accurate analytical model is developed using the Finite Difference Time Domain (FDTD) method for CMOS gate driven coupled *RLC* interconnect line. The model is compared against HSPICE simulations and it is shown that both transient waveforms are matched closely and the average is within 7% for crosstalk and delay estimation. Traditionally, in crosstalk noise modeling, the CMOS driver is modeled as a linear resistor. It is observed that during the transition time transistor operates in linear region as well as saturation region. The percentage of time in saturation region is about 50%. Thus assuming that transistor operates in linear region during the input transition leads to severe errors in noise modeling. Kaushik [B. K. Kaushik and Sankar Sarkar, IEEE Tran. 27, 1150-1154, 2008] proposed a model for crosstalk analysis by considering the non-linear effects of CMOS driver, but this model is limited for coupled two lines.

In this work, CMOS driver is modeled by alpha-power law model and coupled *RLC* interconnect line has been analyzed using the FDTD method [Xiao-Chun Li, Jun-Fa Mao and M. Swaminathan, IEEE Tran. 30, 574-583, 2011]. Using suitable boundary conditions an exact mathematical model for dynamic crosstalk analysis of coupled two interconnect lines is developed. This model gives the accurate results and it can be extended to coupled multiple lines with a minimum computational effort. This paper analyzes propagation delay under the effect of crosstalk using coupled two line architecture as shown in Fig. 1. The analysis for signal integrity is carried out at the global level on-chip interconnects using 130nm technology node. In our experiments, for the equal drive strength of MOS drivers, PMOS and NMOS width ratio is chosen as 2.1. Transient voltage responses of coupled lines with an edge-triggered input are analyzed. The proposed model predicts the propagation delay and crosstalk noise peak with good accuracy as shown in Table 1 and Fig. 2.

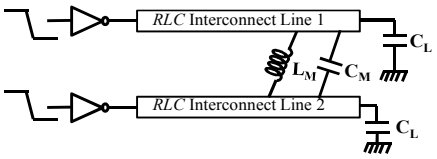

Fig. 1. Coupled two line architecture

Table 1. Delay and crosstalk comparison

Crosstalk induced delay (ps)	**HSPICE**	**CMOS driver**	**% error**	**Resistive driver**	**% error**
Functional	52.5	49.6	5.5	43.7	16.8
In-phase	43.5	42.7	1.8	34.8	20
Out-phase	81.6	77.0	5.6	72.8	10.8
Crosstalk noise peak voltage (V)					
Functional	0.27	0.29	7.4	0.36	33.3

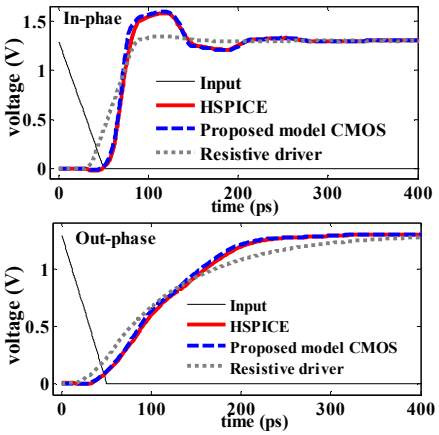

Fig. 2. Transient response of line 1