A 130nm CMOS low power receiver dedicated to Software Defined Radio (SDR) applications

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The number of wireless communication applications has drastically increased during the 2000s and the radio frequencies spectrum, as well as resources, has started to get scarcer. As the time to market is much faster, it's now not possible to produce a new chip every six months for a new specific application. That's why the concept of Software Defined Radio (SDR), introduced by John Mitola in 1992, is interesting. It claims a receiver architecture which is able to convert and digitize the radio frequency signal directly after the antenna, while performing the data processing (channel selection, filtering, demodulation…) in the digital domain. An infinite number of applications can be treated, just by reconfiguring the software and keeping the hardware structure uniform. Of course, this solution is far from realizable, given the state of art of CMOS analog-to-digital converters (ADC), but the rapid evolution of silicon technologies permit now to implement system-on-chip (SoC) systems approaching the ideal concept of SDR, using specific signal processing techniques.

In our work project, we have developed and realized a low power receiver for lower GHz frequencies range, using the N paths filtering concept (L.E. FRANKS and I.W. SANDBERG, The Bell System Technical Journal, vol. 39, pp. 1321-1350). This old technique consists of sampling the RF signal of frequency F_{RF} on N identical paths, acting as time-invariant network characterized by a specific transfer function. By the using of RC elements, it is possible to implement band-pass like transfer function at multiples of the clock frequency $F_{LO.}$ For the generation of the N sampling phases, the clock signal of frequency F_{LO} and duty-cycle D=1/N must be generated by a square pulse signal whose frequency is at least N/2 times the F_{LO} frequency. Just by switching the F_{LO} frequency, we can select a multitude of frequency bands with embedded band-pass filtering, thus reinforcing the linearity and ability of the receiver to receive strong out-of-band blockers. Theses advantages are very interesting and make this technique promising for the future generation of SDR and cognitive radio receivers.

For our 130nm CMOS receiver, we used N=4 paths for sampling the RF signal and each is constituted by a pass transistor with a resistance R_{ON}=54Ω and a capacitor C=10pF. With duty-cycle D=25%, the bandwidth is defined as 10MHz. The -0.9dB conversion gain is 3dB better than classical mixer using 50% duty-cycle and the noise factor is less than 4dB due to the 15dB gain low noise amplifier. Due to the passive mixer structure used, very low power is consumed, while still permitting good performances in linearity and flexibility. Our receiver consumes less than 10mW at 1.2V (including both analog and digital parts) and is functional between 400MHz and 1.5GHz.