

# A 3.88-dB NF 60-GHz CMOS UWB LNA with 14.1-mW DC Power Consumption

Jen-How Lee, and Yo-Sheng Lin

Department of Electrical Engineering, National Chi Nan University, Puli, Taiwan, R.O.C.  
Tel: 886-4-92912198, Fax: 886-4-92917810, Email: [stephenlin@ncnu.edu.tw](mailto:stephenlin@ncnu.edu.tw)

In transceiver design, LNA is a critical block, which receives signals from antenna over the whole band of interest and then amplifies them with a good signal-to-noise ratio (SNR) property. The basic requirements of an LNA include good input impedance matching ( $S_{11}$ ) and reverse isolation ( $S_{12}$ ), high forward gain ( $S_{21}$ ), low NF and high power linearity (or phase linearity) over the whole band of interest, and low power consumption ( $P_D$ ). Recently, several excellent 60-GHz-band CMOS LNAs have been reported [1]-[3]. However, the overall performances of these LNAs are not satisfactory. In the current work, in order to demonstrate that low power dissipation ( $< 15$  mW), high  $S_{21}$  ( $> 10$  dB), low NF ( $< 4$  dB) and excellent phase linearity (i.e. group delay variation smaller than  $\pm 15$  ps) can be achieved simultaneously for a 60 GHz LNA by using a relatively cost-effective 90 nm CMOS technology, we report a low-power, high gain and low NF 60 GHz LNA with excellent phase linearity using a standard 1P9M 90 nm CMOS technology provided by a commercial foundry.

The 60 GHz LNA was designed and implemented in a 90 nm CMOS process. The interconnection lines and the inductors were implemented with the 3.4- $\mu\text{m}$ -thick topmost metal to minimize the resistive loss. The cut-off frequency ( $f_T$ ) and maximum oscillation frequency ( $f_{\text{max}}$ ) of the input transistor  $M_1$  are 95.6 GHz and 136.2 GHz, respectively. The good  $f_T$  and  $f_{\text{max}}$  performances of the transistor indicate that it is possible to apply this CMOS process on the implementation of a high-performance 60-GHz LNA. To achieve sufficient forward gain and reverse isolation, the LNA was composed of a CS stage followed by a cascode stage and a CS stage. To maximize the 3 dB bandwidth of  $S_{21}$ , the output of each stage was equivalently loaded with a low-Q RLC parallel resonant circuit. Over the 60 GHz band of interest, the resonant frequency of the output of the first and third stage is close to the lower corner frequency, while that of the second stage is close to the higher corner frequency. Based on the methodology in [4], simultaneous input impedance and noise matching over the 60 GHz band of interest were achieved by appropriately selecting the values of  $TL_1 \sim TL_7$  as well as the size and bias of the input transistor  $M_1$ , i.e.  $C_{\text{gs}1}$  and  $g_{\text{m}1}$ . In this work, the input transistor has gate-length of 0.1  $\mu\text{m}$ , gate-width-per-finger of 3  $\mu\text{m}$  and finger-number of 13. The extracted  $C_{\text{gs}1}$  and  $g_{\text{m}1}$  are 32.4 fF and 23 mS, respectively. As a result, the LNA exhibited high and flat  $S_{21}$ , small group delay variation and excellent NF at the same time.

The chip area of the LNA is only  $0.591 \times 0.741$  mm<sup>2</sup> excluding the test pads. On-wafer S-parameters and NF measurements were performed by Agilent E8361A network analyzer and Agilent N8975A noise figure analyzer, respectively. The LNA was biased at the condition of  $V_{d1} = 1.2$  V,  $V_{d2} = 1.5$  V,  $V_{d3} = 1.2$  V,  $V_g = 0.56$  V,  $I_{d1} = 3.6$  mA,  $I_{d2} = 3.4$  mA and  $I_{d3} = 3.9$  mA. That is, the power consumption of the LNA is 14.1 mW. The LNA achieves  $S_{11}$  better than  $-10$  dB for frequencies 55.1~59.5 GHz,  $S_{22}$  better than  $-10$  dB for frequencies 55.1~59.4 GHz, and group delay variation smaller than  $\pm 13.25$  ps for frequencies 50.4~63 GHz, an excellent phase linearity result for a 60 GHz CMOS UWB LNA. Additionally, the LNA achieves high and flat  $S_{21}$  of  $9.9 \pm 1.5$  dB and low  $S_{12}$  of  $-42.6 \sim -59.8$  dB for frequencies 50.4~62.9 GHz. That is, the corresponding 3-dB bandwidth is 12.5 GHz. Furthermore, the LNA achieves minimum noise figure (NF) of 3.88 dB at 55.5 GHz and NF of  $4.73 \pm 0.85$  dB for frequencies 50~63.5 GHz, one of the best NF results ever reported for a 60 GHz CMOS LNA. Furthermore, it has been shown that stability factor  $\mu$  or  $\mu' > 1$  is necessary and sufficient for a circuit to be unconditionally stable. The measured result shows the LNA was unconditionally stable for frequencies 0-67 GHz.

A summary of the implemented CMOS LNA, and recently reported state-of-the-art 60-GHz-band CMOS LNAs has also done. Compared with other work, our LNA exhibits not only low power consumption but one of the lowest NFs and highest FOMs. The state-of-the-art results of the proposed LNA indicate that it is very suitable for 60 GHz UWB systems.

## References

1. P. Sakian, E. Janssen, A.H.M.V. Poermund, and R. Mahmoudi, "Analysis and Design of a 60 GHz Wideband Voltage-Voltage Transformer Feedback LNA," *IEEE Trans. Microwave Theory and Techniques*, vol. 60, no. 3, pp. 702-713, Mar. 2012.
2. H. H. Hsieh, P. Y. Wu, C.P. Jou, F. L. Hsueh, and G. W. Huang, "60 GHz High-Gain Low-Noise Amplifiers with a Common-Gate Inductive Feedback in 65 nm CMOS," *2011 IEEE RFIC Symposium*, pp. 1-4.
3. S. Pellerano, Y. Palaskas, and K. Soumyanath, "A 64 GHz LNA With 15.5 dB Gain and 6.5 dB NF in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1542-1552, Jul. 2008.
4. H. K. Chen, Y. S. Lin, and S. S. Lu, "Analysis and Design of a 1.6-28-GHz Compact Wideband LNA in 90-nm CMOS Using a  $\pi$ -Match Input Network," *IEEE Trans. Microwave Theory and Techniques*, vol. 58, no. 8, pp. 2092-2104, Aug. 2010.