Modeling Analysis and Implementation of On-Chip CMOS Transformers

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It is well known that monolithic transformers have been widely used in radio frequency integrated circuits (RFICs) for impedance matching, DC isolation, signal coupling, and phase splitting. Some studies have been carried out on the design, modeling, and optimization of integrated transformers such as the small-signal and compact transformer models for four-port transformers in (Y. S. Lin, *et al*, *IEEE EDL*, 26(3), 208-211, 2005; and J. R. Long, *IEEE JSSC*, 35(9), 1368-1382, 2000). However, similar to silicon-based spiral inductors, on-chip CMOS transformers also suffer from serious power losses at high frequencies, contributed by all metal traces and substrate eddy current effects.

In this work, a set of circular transformers were designed and fabricated on a silicon substrate using standard CMOS technology. To accurately capture the performance parameters of these transformers, we proposed an equivalent lumped circuit model, as shown in Fig.1. Based on the two-port S-parameters measured using standard de-embedding procedure, the frequency-dependent parameters were extracted, including the self-inductance (L_{s1} , L_{s2}) and -resistance (R_{s1} , R_{s2}) of the primary and secondary coils, and the mutual coupling inductance M_p *etc*. Further, the maximum available gain $G_{\max}$, power loss, and minimum noise figure $NF_{\min}$ of these transformers were characterized and compared, which are very useful for the design of certain RFICs.

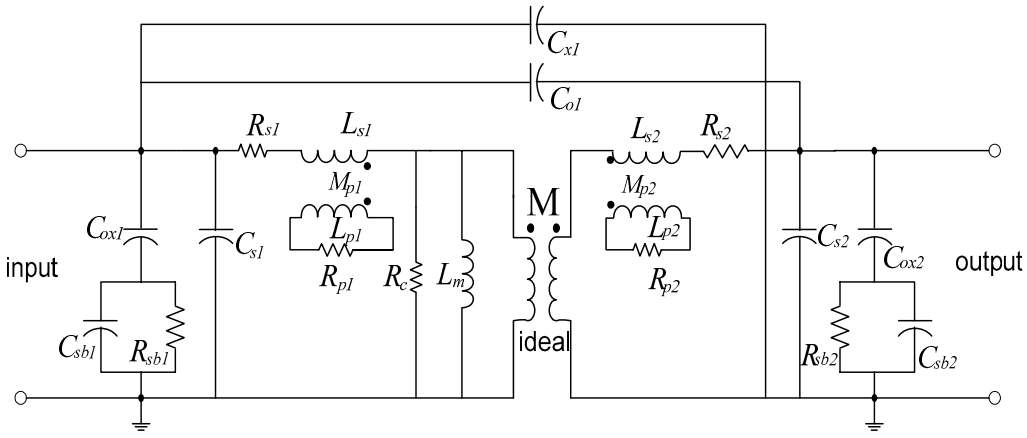

Fig.1. A modified compact model of circular transformer.