Boundary Integral Equation-Based Rapid Design Iterations for Microelectronic Circuits

Swagato Chakraborty and Vikram Jandhyala
Department of Electrical Engineering, University of Washington, Seattle, WA 98195
E-mail : {swagato,jandhyala}@ee.washington.edu, Ph: 206-543-2186 Fax: 206-543-3842

Electromagnetic effects are prevalent in modern day microelectronic circuits due to high-speed and high packing density. In order to maintain desired reliability in low-power and high-performance microelectronic circuits, it is becoming essential for microelectronic circuit designers to use electromagnetic simulation tools even within the design cycle and not merely for verification. Boundary element method (BEM) (S. Rao, D. Wilton and A. Glisson, IEEE Trans. AP - 30, 409-418, 1982) based tools are particularly relevant for prevailing planar multilayered circuits. Design iterations, wherein sub-circuits or components are iteratively modified in order to achieve a desired design goal, require especially efficient EM simulation methods owing to the repeated computations needed.

This paper presents a technique to speed up BEM-based electromagnetic simulation design iterations. The technique relies on the surface equivalence principle to isolate the region where a component or sub-circuit is being designed. By this isolation, the section under design interacts via Green's functions only with the enclosing surface. This surface, in turn interacts with the remainder of the geometry. The advantage of this separation into an exterior and interior problem is that the overall BEM matrix requires a significantly smaller modification from one design iteration to the next. In an original BEM system, the sub-matrix representing the self interaction of the section under design, as well as rows and columns modeling the interaction between this section and the entire geometry are all modified. Conversely, in the interior-exterior approach, the modified section of the matrix is the self interaction matrix and the interaction of the section under design with the surface only. The surface itself does not scale as the overall problem size and is typically much smaller than the overall problem and also simpler or smoother than the section under design.

This work extends the original work (S.Chakraborty and V.Jandhyala, EPEP-'04, 45-48, 2004) to the general and useful case of touching subsections of conductors as opposed to explicitly isolated and separated components.

Examples shown at the conference will include inductor design, inductor-trace coupling, and coplanar waveguide design and in particular for filter design. The Schur complement technique is used to accelerate the overall solution and reuse both setup and inversion steps to obtain dramatic speedups of two to three orders of magnitude for realistic design iterations using direct solvers.