

Improved Fast Hierarchical Algorithm for 3-D Capacitance Extraction

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Electrical performance of interconnects is increasingly important for high-speed integrated circuits. Accurate determination of signal propagation characteristics along interconnects represents a crucial design problem. The need for accurate interconnect models has become essential to chip and system design. Much work has been directed at rapidly solving for the capacitance or inductance of three-dimensional (3-D) interconnects. Recently, a fast hierarchical algorithm has been introduced for 3-D capacitance extraction (W. Shi, J. Liu, N. Kakani, and T. Yu, IEEE Trans. CAD, **21**(3), pp. 330-336, March 2002). The fast hierarchical algorithm was based on a hierarchical algorithm for the n -body problem and is an acceleration of the boundary element method (BEM) for solving the integral equation associated with the capacitance extraction problem. It was shown that the fast hierarchical algorithm is much faster than FastCap and uses much less memory than FastCap (Fastcap: K. Nabors, S. Kim, and J. White, IEEE Trans. MTT, **40**(7), pp. 1496-1506, July 1992).

In this work, an improved fast hierarchical algorithm is introduced for the 3-D capacitance extraction. This new algorithm includes two major improvements. Firstly, an enhanced hierarchical partition (or refinement) algorithm is introduced by adopting a new scheme for partitioning conducting surfaces. The calculation precision is greatly increased by the use of the new hierarchical partition algorithm. Secondly, improved hierarchical data structures are proposed for enhancing the performance of the acceleration. The new hierarchical data structures fully exploit the acceleration nature of the fast hierarchical algorithm and thus can give a further speedup in 3-D capacitance extraction. Numerical examples to demonstrate the performance and efficiency of this newly enhanced fast hierarchical algorithm are included.