Effects on CMOS and TTL due to HPM-Signals

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Systematic measurements of thresholds values for upset or damage of electronic components and their interpretation provide valuable information for both source developing and for hardening measures of systems.

This paper presents measurements of upset and damage of digital electronic components (CMOS and TTL) due to exposure to MW-signals and the interpretation of the data from more than 800 samples.

To measure the performance of electronic components (DUT) when stressed by MW-signals a setup was designed and tested which allows a well-defined voltage signal to enter the component during normal operation, and to discriminate its effect on the component. During the measurements the input current into the DUT and the DUT-current are continuously monitored, as well as the logical performance of the DUT itself. Based on variation of voltage level, pulse width, and stress mode (single and repetitive shot) an algorithm was developed to describe the effect of these parameters on the threshold level.

The results show a remarkable statistical reproducibility for each individual type of DUT, significant differences between different types of the same family and – with respect to the parameters varied – a wide range of components being rather sensitive to the voltage level or the energy of the threat. The influence of repetition, i.e. the number of pulses per voltage level, seems to be dominant for those components which do not clearly belong to either the “voltage sensitive” or “energy sensitive” group. The study is completed by experiments describing the damage mechanism of a TTL.