Full-wave modeling of the impact of the semiconductor substrate on on-chip electromagnetic interference and power distribution network performance

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In RF and mixed-signal integrated circuits (ICs) the underlying semiconductor substrate forms a distributed coupling path, through which spurious currents produced from the switching activity of various electronic components can be transmitted and result in undesirable interference. These currents are injected into the substrate mainly through the parasitic capacitances of the junctions of electronic devices with the substrate and through the parasitic inductances of the power delivery network and the package. Their presence in certain blocks of digital circuits and close to sensitive analog components entails the possibility of system performance degradation or even malfunction. For this reason, there has been a considerable effort over the past several years to model, quantify and analyze the problem of substrate noise coupling. So far, the emphasis of this modeling effort has been on the quasi-static analysis of the problem, which leads to the extraction of an equivalent RC network representation of substrate noise coupling. This has been a reasonable approximation for frequencies such that dimensions of the IC functional blocks comprise a very small fraction of the wavelength. Yet, with the operating bandwidth in state of the art ICs and the ones projected for future implementations extending to multiple tens of GHz, it is necessary to reconsider the accuracy of the RC models by quantifying and analyzing the full-wave attributes of semiconductor-induced coupling between remote blocks of circuits. Towards this end, the Method of Moments (MoM) is used in this paper to solve the full-wave mixed potential integral equation for the quantification of electromagnetic coupling between contacts on top of the multilayer semiconductor substrate. A qualitative and quantitative comparison between the full-wave results for the mutual impedances between properly defined ports with those obtained from the quasi-static analysis provides for a frequency-dependent assessment of the importance of electrodynamic effects for the case of the most commonly used substrates in RF and mixed-signal ICs.

The presence of the lossy semiconductor substrate affects additionally the response attributes of the on-chip power supply network. The impact is mostly beneficial in terms of lower voltage swings during switching. Accurate prediction of this impact is needed in conjunction with the accurate estimation of on-chip decoupling capacitance needs to avoid overdesign and wasting of valuable chip real estate. A versatile and powerful method for on-chip power supply modeling is the FDTD method. Obviously, when the FDTD grid extends over a volume containing the underlying substrate, its impact would automatically be incorporated in the final results. However, the substrate volume tends to be much larger than the volume containing the power grid, thus leading to a dramatic increase of the computational resources needed for the FDTD modeling. This extra computational burden on the FDTD simulations can be avoided through the implementation of accurate surface impedance relationships to serve as behavioral models for the effects of the semiconductor substrate. Such an FDTD-compatible macromodeling of the semiconductor substrate is also developed and discussed in this paper. The pertinent, frequency-dependent, surface impedance macromodel is expressed in terms of a spatial convolution integral relationship between the tangential electric and magnetic fields on the semiconductor substrate surface, involving an appropriately-constructed Green's function. For the discrete model this relationship is in terms of an impedance matrix. Use is made of a broadband fitting algorithm to cast the frequency-dependent impedance matrix elements in terms of closed-form rational functions of frequency. In this manner, recursive convolution practices can be employed for the computationally efficient incorporation of the equivalence surface impedance model in the FDTD algorithm.