FPGA-based Data Acquisition and Beamforming System For UWB See-Through-Wall Imaging Radar

Yunqiang Yang*(1), Jianye Wang(1), Shaoyu Liu(1),
Mohamed Mahfouz(2), Aly E. Fathy(1)
(1) Electrical and Computer Engineering Department
(2) Mechanical, Aerospace and Biomedical Engineering Department
University of Tennessee, Knoxville, USA

We have developed an ultra-wideband see-through-wall imaging radar system, its FPGA data processing, and beam-forming network. Our studies have included: UWB 1D/2D array designs, wall effect on microwave image quality, high-resolution UWB image formation method, and real-time data processing. Both theoretical and experimental data have been collected.

Theoretically, the quality of see-through-wall imaging microwave radar systems is generally poor, and it is always desired to improve its resolution. There are several approaches to improve this image quality, such as utilizing advanced computationally intensive imaging algorithms, and implementing large-aperture array. The implementation of image formation algorithms has also to consider diffraction effects due to the complicated see-through-wall scenarios. In our study, we have identified various systems tradeoffs and our developed algorithm has been significantly improved based on taking into account these effects. In addition, a series of finite difference time domain study cases have been analyzed using conformal finite difference time domain analysis tool (CFDTD). As an outcome of such study, an extensive library has been developed based on the simulation of different object types. This library can be used to develop a pattern recognition capability.

Experimentally, we needed to develop a low cost high-speed data acquisition network and a high performance digital beam-forming processor. The data acquisition network is a key subsystem that interfaces between the developed UWB synthetic aperture array and the onboard digital beam-forming radar processor. Digitization of UWB signal normally requires custom design of analog-to-digital-converters (ADC) with intensive wide bandwidth and fast sampling speed. Hence, we implemented a cost-effective data acquisition network, based on the sequential equivalent-time sampling technology, using both a relatively low-speed *Maxim* ADC and a high performance Field-Programmable-Gate-Array (*FGPA*). For handling the image formation this unit is followed by an FPGA-based Digital Beam-forming Processor (DBP). The core functions of the *DBF* have been designed in the *VHDL* (Very-high-speed-integrated-circuit Hardware Description Language) and are implemented onto a high-density *Xilinx Virtex* IV *FPGA*. This novel design can achieve real-time processing for high-resolution imaging and tracking modes of the radar system. The principles and algorithms of the array beam-forming are based on an UWB pulse model and will be discussed in this paper; as these very encouraging results will help in meeting the real-time and high-resolution processing demands.