Development and Application of Physics-based Compact Models for High-Impedance Electromagnetic Surfaces Integrated in a Power Plane Configuration

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Abstract: Physics-based compact models for the unit cell of power planes with integrated high-impedance electromagnetic surfaces are developed and cascaded in a two-dimensional array to build full models for large and multi-layer power planes. The compact model offers a significant advantage to the FEM-based electromagnetic simulation as it reduces the analysis time of a typical 10cmx10cm power plane from 40 hours to less than 10 seconds. The proposed compact model is also used to explore the noise mitigation at different locations of the power plane and in combination with RC decoupling for broadband noise mitigation.

I. INTRODUCTION

With the increase in gate density and the reduction in supply voltages, modern microprocessors are more vulnerable to signal integrity issues. Since active devices on a modern computer may have switching frequencies varying from a few hundred MHz to about 2 GHz, it is imperative that new solutions be found for broadband simultaneous switching noise (SSN) mitigation. With most of the switching noise being concentrated at the first harmonic of the clock frequency, an ideal noise mitigation bandwidth should expand from a few hundred MHz to 4GHz. Until today, the most common approach to SSN mitigation remains the use of decoupling capacitors to suppress the resonant modes of the power planes, which behave as a parallel-plate waveguide [1]. This approach, however, is very limited because it offers only localized solutions. In addition, it is efficient only up to 700 MHz for a 10cmx10cm power plane for example [2].

A novel approach has recently been proposed for resonant modes suppression in parallel-plate waveguides and is applicable to power planes as well. This concept consists of replacing one or both plates of the waveguide with a high-impedance electromagnetic surface (HIS). Full wave analysis [2], [4] and experimental characterization reported in [3] have shown that such waveguides can be designed to mitigate parallel-plate resonant modes at frequencies as low as 700MHz with a wide bandwidth extending in the low Gigahertz range. Electrical equivalent circuits of these novel power planes are necessary for their use in full package simulators such as PSPICE. The only model reported so far for stand-alone HIS with rectangular patches is based on the transmission line theory and is limited to two main directions of wave propagation [5]. In this work, we propose to develop a lumped-element compact model for these novel power planes. This model should be physics-based and generic enough to apply to power planes of any size with single or multiple layers. The geometry of the power plane is first reviewed. The development, validation and application of the compact model are then discussed

II. POWER PLANE GEOMETRY

Figure 1 shows a typical power plane with integrated HIS, where the bottom plate or ground plane of the traditional power plane has been replaced with a HIS. The HIS has the ability of stopping surface wave propagation on a given frequency band [6]. It consists of polygonal metallic patches connected to a bottom metallic plate through straight metallic posts (vias) with square or circular cross section and is filled with dielectric material. The key geometrical parameters of the power plane system include the via to via distance or periodicity (a) of the HIS, the via height (t), the separation or gap (g) between the patches, the patch width (w) and the thickness (d) of the dielectric material between the HIS and the top or V_{DD} plane. While the performance of the power plane system are controlled by varying the above geometrical parameters, a dramatic change in the

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performance is obtained by using either an inductance-enhanced [4] or a capacitance-enhanced HIS [3], [6]. Inductance-enhanced HIS are achieved by replacing the straight via of the simple HIS with a more inductive element such as a spiral or a single loop inductor and are especially important when wideband noise mitigation is desired at very low frequencies. Capacitance-enhanced HIS are obtained by using double-layer patches and are more appropriate for narrowband SSN mitigation.

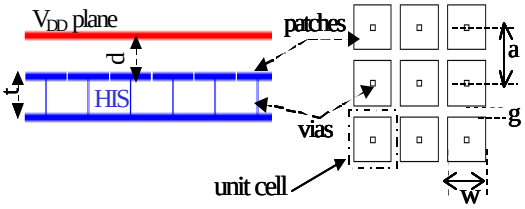

Fig. 1. Geometry of power plane with straight vias Side view (left) and top view (right)

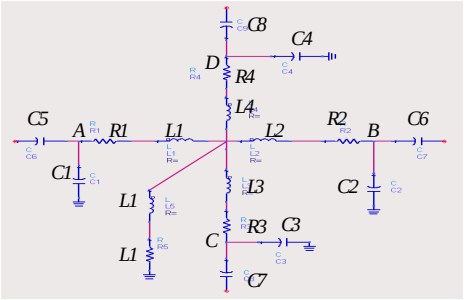

Fig. 2. Compact model of the HIS unit cell

III. COMPACT MODEL DEVELOPMENT

A. Model form definition

The power plane model is developed by first dividing it into unit cells. Each cell is modeled individually and all are then cascaded into a 2D array to construct a full model for the power plane. The boundaries of the unit cell are pre-defined by the periodicity of the HIS. Figure 2 shows the model form for the unit cell of a HIS with square or rectangular patches. The series RL–pairs R1L1 through R4L4 that originate from the center of the patch represent the impedance of the patch. The via is modeled by the RL-pair R5L5. The capacitors C1-C4 model the capacitive coupling between the patch and the bottom metallic plate. The capacitors C5-C8 model the capacitive coupling to the adjacent cells.

Figure 3 shows the full model of the power plane unit cell, obtained by connecting the top plate and HIS unit cells at nodes A-D. In this mode, the section of the V_{DD} plane directly above the HIS unit cell is modeled with the series RL-pairs R6L6 through R9L9. The capacitors C9-C12 represent the capacitance between the top plate and the patch. This compact model form is very generic and can be used for power planes with inductance or capacitance-enhanced HIS as well. In general, when the polygonal patch has n sides, the number of series RL-pairs originating from the center of the patch is equal to n. The coupling capacitors to ground and to adjacent patches are available on each side of the unit cell as discussed earlier for the case of rectangular patches.

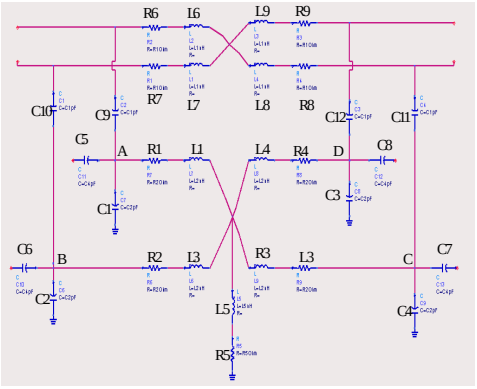

Fig. 3. Compact model of the power plane unit cell

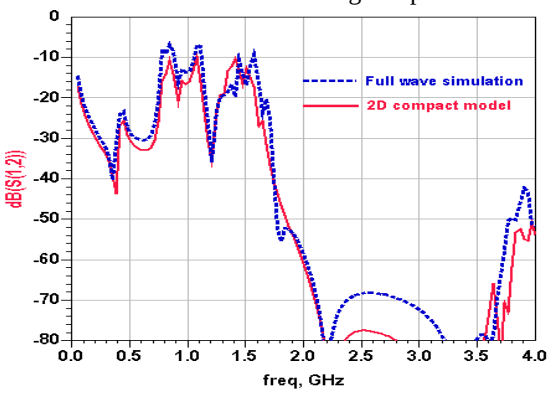

Fig. 4. Modeled vs. simulated S12 of plane 1

B. Compact Model Validation

The model extraction occurred in three steps. First, S-parameters are generated for the solid 3D model using the finite element method (FEM) code HFSS [7]. Second, initial values are assigned to the compact model using existing formulas for thin film inductors and parallel-plate

waveguides [8]. Finally, the model component values are refined using optimization routines implemented in the commercial tool Agilent-ADS [9]. For the validation of the model and further analysis in this document, we will consider only two power planes denoted plane 1 and plane 2. Plane 1 is a 9cmx10cm power plane. The HIS has 1.54mm high vias and square patches with periodicity of 1cm. The separation between the patches is 400um and the distance between the HIS and the Vdd plane is 1mm. Plane 2 is a 10cmx10cm power plane. The HIS is inductance-enhanced by using a single loop inductive element of length 16mm. The total thickness of the power plane (including HIS) is 1.54mm and the spacing between the patches is 400um.

Figure 4 shows the simulated vs. modeled insertion loss of power plane 1. The noise source (port 1) is located at (4.5cm, 4.5cm) and the load (port 2) is located at (4.5cm, 1.5cm). A good agreement is obtained over the frequency range of interest.

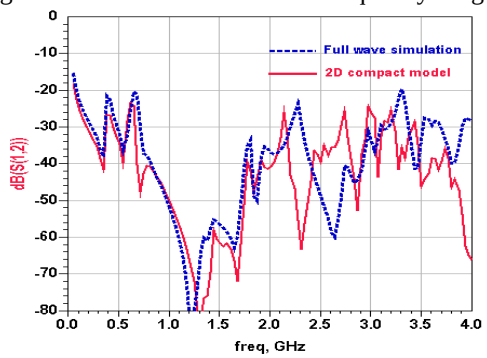

Fig. 5. Modeled vs. simulated insertion loss of plane 2

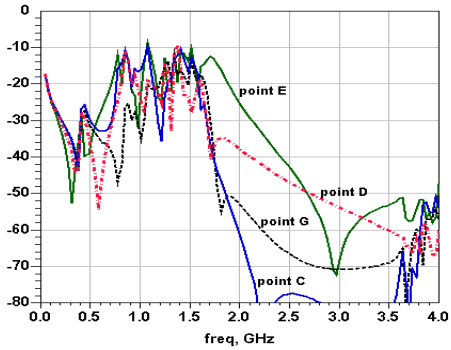

Fig. 6. Insertion loss of plane 1 for different noise source to load distances

Figure 5 shows the modeled vs. simulated insertion loss (S12) of power plane 2. Port 1 and port 2 are located at (4.5cm, 4.5cm) and (4.5cm, 1.5cm) respectively. A good agreement is obtained from DC to the upper edge of the stopband. Above the upper edge, the two curves have the same shape, with a frequency (phase) shift of about 0.4GHz between simulation and modeling. This discrepancy can be adjusted by additional tuning of the model component values.

IV. COMPACT MODEL APPLICATION

A. Noise mitigation at different locations on the power plane.

The compact model defined above can now be used in a circuit simulator for the analysis of the noise mitigation capability of the power plane system. Since the model is physics-based and periodic, its validation is not restricted to the position of the load and noise sources as defined in the reference full wave simulation used to extract the model component values.

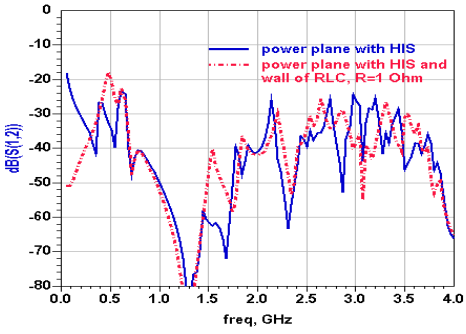

Fig. 7. S12 of plane 2 with and without series RLC at its edges

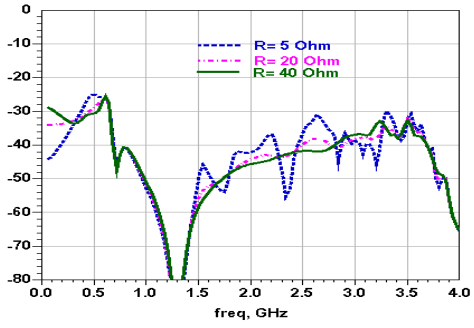

Fig. 8. Effect of shunt resistance on SSN mitigation on plane 2

To study the position dependency of the noise mitigation we consider power plane 1. First the noise source (port 1) was fixed at point A (4.5cm, 4.5cm) and the load position varied through the points ED-G-C of coordinates (4.5cm, 3.5cm), (4.5cm, 2.5cm), (4.5cm, 1.5cm) and (4.5cm, 0.5cm) respectively. The resulting insertion loss (S12) is plotted in figure 6. When the receiving port is closest to the noise source the minimum insertion loss in the stop band increases, indicating

the presence of leaky modes. As the distance increases, the bandgap converges to a fixed width with a simultaneous increase in the signal transmission at low frequencies. This would be a drawback for this approach if there were active devices on the board switching in the 500-700MHz-frequency range. In this case the use of a power plane with inductance-enhanced HIS is necessary as it extends the lower cutoff frequencies, while keeping a reasonably wide stopband.

B. Combination of HIS with decoupling capacitors

Resonances due to the wave reflection at the edge of the finite width power plane can be mitigated using decoupling capacitors between the V_{DD} and the ground planes around the perimeter of the power planes. This technique is applicable to both traditional power planes and power planes with integrated HIS. Figure 7 shows the insertion loss of power plane 2 with and without decoupling capacitors. A substantial attenuation of the transmission coefficient is achieved at very low frequencies with decoupling capacitors. Here each decoupling capacitor is modeled as a series RLC, with C being the desired decoupling capacitance, L the associated lead inductance and R a resistance (generally) selected to match the impedance of the parallel plate waveguide without HIS.

Figure 8 shows the insertion loss of power plane 2 with 40 decoupling capacitors (RLC) placed around the perimeter. This corresponds to a capacitor density of one capacitor/cm. The resistance R is varied from 5 to 40 Ohm, with L and C fixed at 1nH and 0.5nF respectively. The resonant mode attenuation improves at high frequencies as R increases, but at the same time there is a small degradation of the resonant mode mitigation at low frequencies.

V. CONCLUSIONS

A lumped-element compact model has been developed for power planes with integrated high-impedance electromagnetic surface. The compact model is based on the unit cell approach and can be expanded to model power planes with different sizes and single or multiple layers. The model was validated on power planes with simple and inductance-enhanced HIS. Good agreement was obtained between the modeled and the simulated S-parameters over the frequency range of interest. The compact model offers a significant advantage to the FEM EM simulation as it reduces the simulation time of a typical 10cmx10cm power plane from 40 hours to less than 10 seconds. The compact model was also used to study the noise propagation over the entire board and to determine the requirements on decoupling RC networks for broadband SSN mitigation.

ACKNOWLEDGMENT

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