

# Comparative Studies on the Capacitive Coupling in 3D Interconnects Embedded in LTCCs

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**Abstract:** It is known that high-performance printed circuit boards (PCBs) consist of multi-layer materials with multiple signal microstrips embedded within. The high-density integration has made the overall signal integrity analysis a very important work. Signal integrity usually include signal delay, distortion, and crosstalk, which are the manifestation of the mutual inductive and capacitive couplings among all microstrips.

To the authors' best knowledge, till now much work has been done for extracting the microstrip capacitances and inductances in three-dimensional (3D) interconnects. Some empirical capacitance models for 2D and 3D interconnects are developed ( T. Sakurai, *IEEE Trans. Electron Device*, **ED-40**, 118-124, 1993; S. –C. Wong *et al*, *IEEE Trans. Semi. Manufact.*, **SM-13**, 108-111 and 219-227, 2000). However, most of these work was focused on the interconnects fabricated in U(V)LSIs, and only Sohn *et al* have given a set of empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in normal printed circuit boards(Y. S. Sohn *et al*, *IEEE Trans. Advanced Packaging*, **AP-24**, 521-527, 2001).

In this work, comparative studies on the capacitive coupling in 3D-interconnects embedded in LTCCs (Fig. 1) are done, including the hybrid effects of various geometrical parameters of both microstrips and LTCC superstrate-substrates. The accuracies of different empirical formulas for predicting the capacitive coupling in 2D and 3D interconnects on PCBs are examined and compared. Some conclusions are drawn, which are very useful for practical PCBs design for improving the signal integrity.

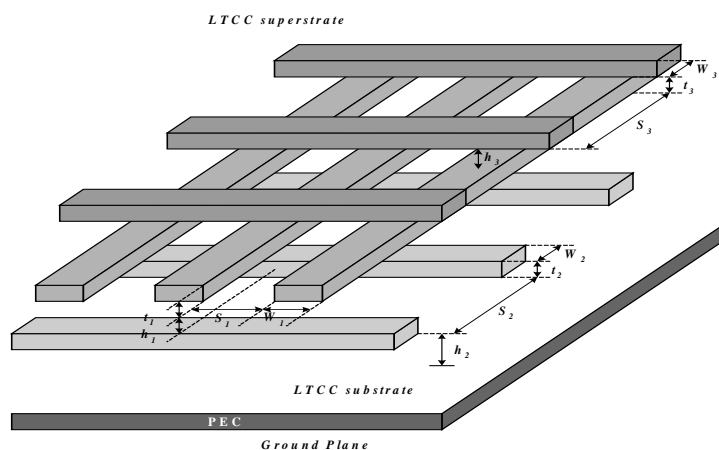


Figure 1. Three-dimensional interconnect embedded in a LTCC superstrate-substrate.