Signal Integrity Issues for Package Level Discontinuities and RF Chip-Package Interconnects Using FDTD Analysis and Equivalent Circuit Modeling

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As on-chip frequencies move into the gigahertz region a need exists to gain an understanding of how interconnects impact signal integrity. Signals can be degraded by discontinuities along the signal path as well as coupling from adjacent circuits. There are several established methods to analyze the effects of discontinuities and coupling. These include both full wave simulations and equivalent circuit models. These circuit models are typically developed for a particular layout and are optimized to obtain element values to match the response of a full wave simulator. One drawback of this method is re-optimization is required for a different geometry. The current work develops an equivalent circuit model to estimate coupling using closed form equations. The major advantage is that changes in the geometry are accounted for in the equations and no tedious re-optimization is required. Insight into signal integrity issues can be obtained through time domain analysis. To facilitate this a Finite Difference Time Domain (FDTD) code was written implementing a UPML absorbing boundary for lossy materials.

The structure used for this work is shown in fig. 1, where two vias, rectangular in cross section, are placed a distance d apart (center to center). These vias connect transmission lines of length l_1 and width w_1, on the top layer (solid lines), to transmission lines of length l_2 and width w_2 on a lower layer (dotted lines). This structure was chosen because it exhibits both discontinuity and coupling effects. To develop the equivalent circuit model the length of the coupled vias were divided into two segments. The circuit model for each segment is shown in fig. 2, where L represents self-inductance, R is the losses associated with the vias, and Ca and k represents coupling between the vias.

The S-parameters obtained from the circuit model are compared with that obtained from FDTD and are shown in fig. 3. The model shows very good agreement. Figure 4 shows coupling from port 1 to port 3 and 4 in the time domain, for a 10GHz sinusoidal (2 Vp-p) input applied at port 1. These results show that coupling from neighboring circuits can be significant enough to impact signal integrity thereby degrading system performance.

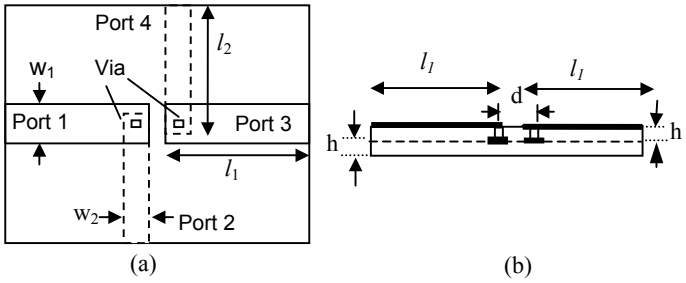

Fig. 1. Coupled via structure. (a) top view (b) side view, w_1 = 11.58 mils, w_2 = 5.79 mils, l_1 = 33 mils, l_2 = 37.89 mils, h = 2.46 mils, D = 7.79 mils, via dimensions = 2 × 2 × 2.46 mil

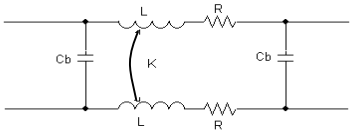

Fig. 2. Equivalent circuit model for a coupled via subsection

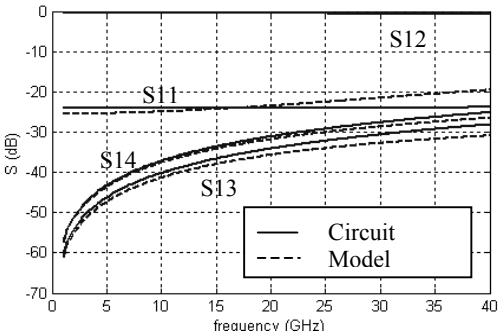

Fig. 3. Comparison of S-parameters for Coupled via structure

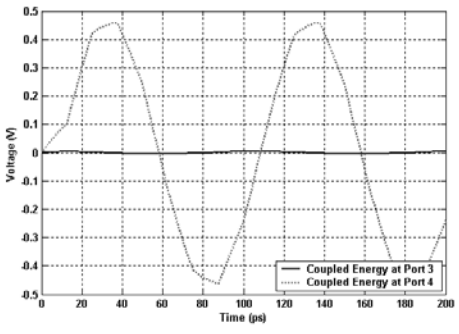

Fig. 4. Time domain coupling for port 3 and 4