DC BIAS EFFECTS ON BULK SILICON AND POROUS SILICON SUBSTRATES

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***Abstract* — The relationship between attenuation and biasing for CPW architectures on bulk and porous silicon films is investigated. Biasing effects on low resistivity silicon can have loss variations as high as 34 dB/cm under negative bias (0 to –10 V) and 2 dB/cm for positive bias (0 to 10 V) conditions. While the inclusion of an oxide film substantially reduces loss variation (< 0.1 dB/cm), the use of a 68 % porous silicon film can provide further stability (< 0.01 dB/cm) in addition to lowered attenuation in the range of 1.3 to 3 dB/cm from 5 to 20 GHz.**

***Index terms* — CPW attenuation, Porous silicon, Bias dependent attenuation**

I. INTRODUCTION

In the last few years, important building blocks have been developed in silicon based integrated circuits to facilitate design in integrated microsystems. Examples of components include sensing elements, high-speed digital processors, and high-speed transceiver designs that are commonly used in broadband communication applications.

As the trend for reduced device size and lower power consumption continues, new expectations for increased device functionality - voice, video, and data - place larger constraints on circuit design formats. Furthermore, as non-traditional low cost RF applications, such as wireless PDA devices, continue to move steadily into the GHz regime, challenges arise to establish trade-off metrics between performance and cost.

The importance of lowering the cost of high performance RF designs has stimulated interest in silicon based material systems. However, between high and low volume applications, performance requirements vary considerably. Hence, there exists an important need to identify methods of design in silicon that can accommodate a broad set of performance and bandwidth conditions. These methods would provide important resources to aide commonalization of functions within a given microsystems comprised of MEMS, RF and digital circuitry.

Porous silicon has the potential to aid in the design of RF microsystems. Attenuation properties show significant promise when compared to bulk low resistivity silicon [1] in CPW architectures of similar aspect ratio. Adjusting film porosity can reduce material properties such as dielectric constant and loss. Porous silicon is therefore capable of providing electrically thick electromagnetic environments which are desirable for antenna fabrication and is complimentary to post-processing CMOS circuits.

This paper presents the results from a study of DC bias effects on printed interconnects onto silicon substrates with varying resistivities. MEMs, active RF, and digital circuits all require different bias conditions. A comparative analysis therefore of RF response is needed to quantify the impact of bias voltage on circuits printed on various forms of silicon substrates. This data is significant for determining the variation in signal behavior within interconnects, as well as, active planar circuit designs.

II. COPLANAR WAVEGUIDE DESIGN

Three types of substrates are compared: high resistivity (> 2000 ohm_cm), low resistivity (10-20 ohm_cm), and porous silicon based on a 10-20 ohm_cm starting silicon material. Most test wafers are <100> orientation and P-type except for the N-type high resistivity wafers. Electrode designs are printed directly onto the bulk silicon substrates with and without a plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide film. This is

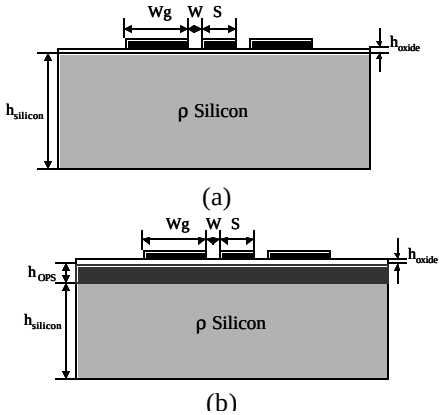

Figure 1 (a) and (b) Cross sectional view of the various CPW structures

Design	Substrate		$h_{silicon}$ (mm)	h_{oxide} (mm)	h_{OPS} (mm)	CPW impedance (ohms) (Maxwell 2D simulation [2])	Circuit dimensions (mm)		
	r ohm_cm	Type					S	W	Wg
CPW A	>2000	N	525	0	0	44	33	18	140
CPW B	>4000	N	406	0.5	0	46	33	18	140
CPW C	10-25	P	510	0	0	44	33	18	140
CPW D	10-25	P	525	0.5	0	46	33	18	140
OPS_CPW A	10-25	P	491	0.5	34	54	47	12	140
OPS_CPW B	10-25	P	503	0.5	22	59	47	12	140

Table 1: CPW architectures

shown in fig. 1a where the CPW line is on a bulk silicon film ($h_{silicon}$) with an oxide film (h_{oxide}). All porous designs are printed onto an SiO_2 capped layer using the method described in [1] with a film thickness of h_{ops} (fig. 1b). Oxide thickness is nominally 5000 Å and all the metal conductors are electroplated Au to a thickness of 4 µm on Ti/Au seed layers. See table 1 for exact details of the designs under study.

The porous silicon samples used in this work have been formed by the anodization of silicon in an HF/Ethanol solution. The porous films are defined according to a volume porosity, where porosity is the ratio of the weight of the porous film to the weight of bulk silicon that occupies a similar volume. Since this quantity is defined by a gravimetric method, the label reflects a volumetric parameter. The two porosities considered are 61% and 68% with film thickness of 22 µm and 34 µm respectively. Note that the nanometer size holes of this medium allow the structures to be evaluated as a homogeneous, although porous material. For a further in depth discussion on this process as it relates to the oxide capped porous silicon on which circuits OPS_CPW A and OPS_CPW B are printed see [1].

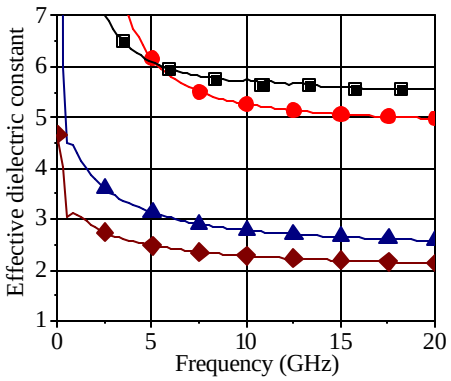

Fig. 2. Effective dielectric constant of various circuit architectures(■= CPW C, ●= CPW D, ▲= OPS_CPW A, and ◆= OPS CPW B)

The designs discussed herein are chosen to have similar aspect ratios. All circuits are designed to have a Re (Zo) of 50 ohms. In the case of porous films, increasing porosity inherently lowers the dielectric constant of the film. A comparison is shown in fig. 2 of the effective dielectric constant for 61% and 68% porosity films to bulk low resistivity silicon with and without an oxide film. These results indicate the type of reduction in effective dielectric constant values that is achievable using porous silicon technology. Typical effective dielectric constant values in bulk silicon are approximately 5.5 and 5 with and without SiO_2 respectively. Much lower values of 2.5 and 2.1 are possible in porous samples for porosities of 61% and 68%.

III. Results and Discussions

Device S-parameter response is measured with an Agilent 8510C automatic network analyzer connected to a Cascade Microtech/Alessi RF1 microwave on-wafer probe station. Cascade Microtech GSG150 probes are used to perform the NIST MultiCal TRL (Through-Reflect-Line) de-embedding calibration [3]. The circuits are each biased with a dc voltage at port 1. Each sample contains distinct TRL calibration circuits. Through experimental verification, calibration with and without biasing did not produce observable change in the measured results. Thus, the TRL calibrations in this work are done with no bias.

Bias effects relative to 0 V condition

Fig. 3a shows the response of a CPW printed on bare high resistivity silicon. For a high resistivity design (ρ > 2000 ohm_cm) positive biasing results in improved attenuation similar to results observed in [4]. An SiO_2 film on a higher resistivity substrate (ρ > 4000 ohm_cm) for similar bias conditions results in more attenuation for positive bias. Note the additional thin film extends the bias potential to +/- 19 V. A low resistivity design on bare silicon, however, displays significant variation (fig. 3c).

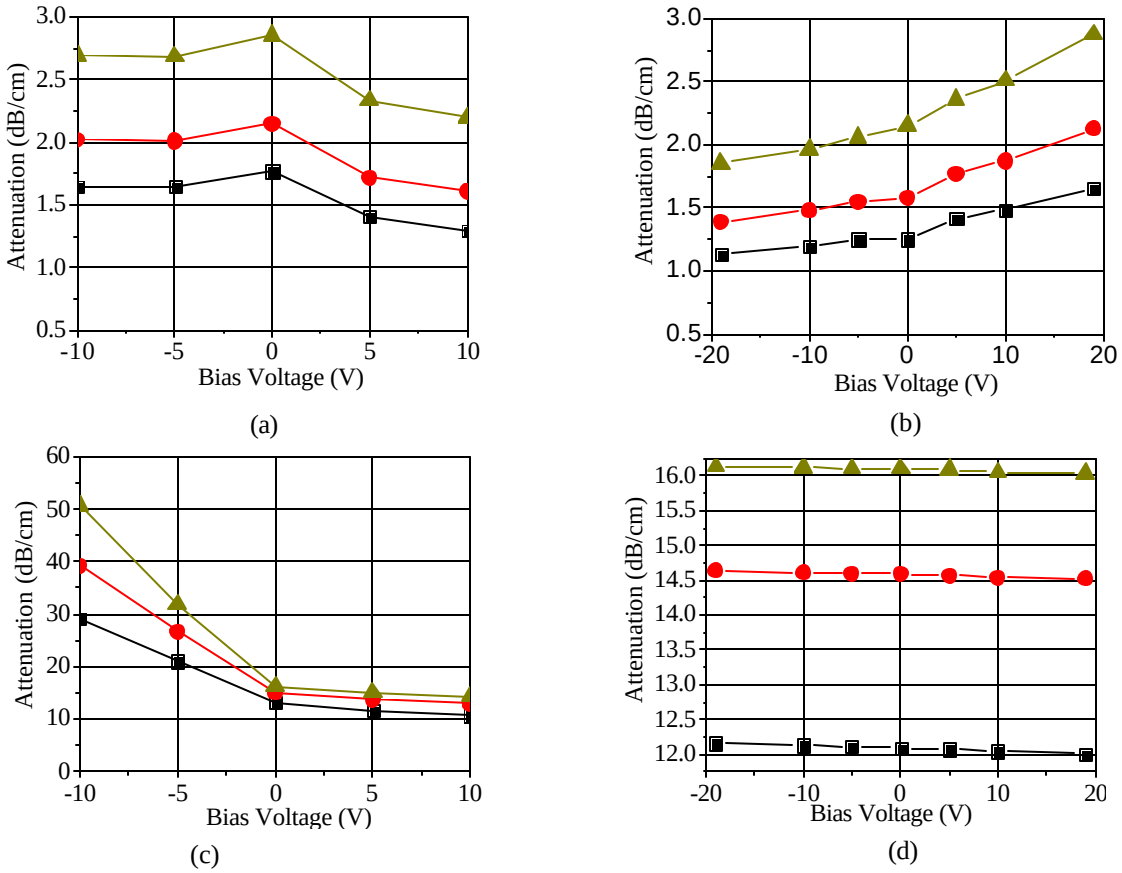

Fig. 3 Attenuation vs Bias voltage at various frequencies (■ = 5 GHz, ● =10 GHz and ▲= 20 GHz) (a) CPW A, (b) CPW B, (c) CPW C, (d) CPW D

The 20 GHz response in the negative bias condition (-10 to 0 V) decreases from 50 to 16 dB/cm whereas under positive bias conditions (0 to + 10 V) the decrease is only 2 dB/cm. The addition of an SiO_2 film significantly reduces the bias effects as seen in fig. 3d to +/- 0.05 dB/cm for larger +/- 19 V bias conditions. The oxide cap, therefore, provides significant isolation in CPW lines on low resistivity when biased.

When the two porous samples were evaluated, further improvement in bias isolation was observed. The lower porosity sample (61% porosity), fig. 4a, has a variation of approximately +/- 0.1 dB/cm (at 20 GHz) with a bias of +/- 19 V, whereas, the higher porosity sample (68%) shows negligible variation (< +/- 0.005 dB/cm) under

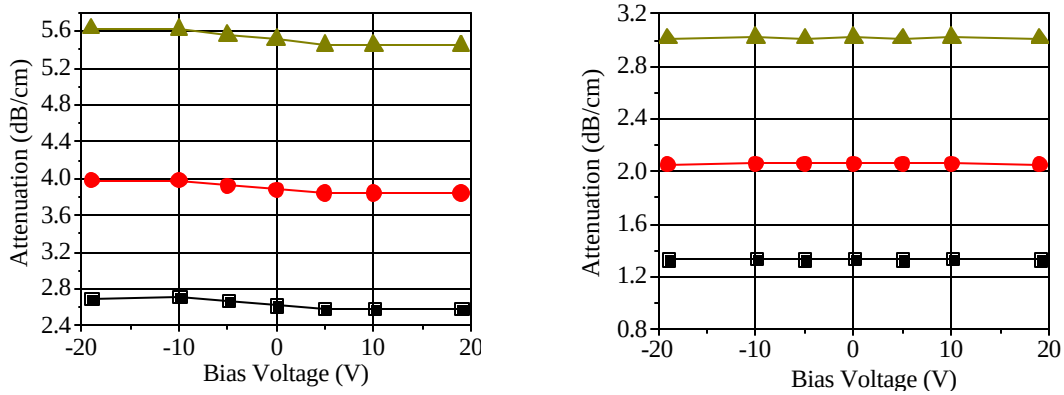

Fig. 4 Attenuation vs Bias voltage at various frequencies (■ = 5 GHz, ● =10 GHz and ▲= 20 GHz) (a) OPS_CPW A, and (b) OPS_CPW B

similar bias conditions. This indicates that the porosity of the porous silicon plays an important role in enhancing the isolation and minimizing the variance in attenuation under varying bias conditions. An added benefit over bulk low resistivity samples is that the porous silicon film significantly reduces the attenuation of the CPW bringing its performance closer to high resistivity designs.

The conductor loss contribution for the various circuits discussed is shown on table 2. All CPW lines on bulk silicon have similar conductor loss as do the two porous circuits. However, the dielectric loss contribution in the porous materials is different based on porosity values and hence, the observable difference in loss. Thus when compared to the bulk high resistivity silicon, the 68% porous silicon sample (OPS_CPW B) fig. 4b has comparable attenuation.

Design	Simulation Frequency (dB/cm)		
	5 GHz	10 GHz	20 GHz
CPW A	0.67	0.97	1.39
CPW B	0.64	0.93	1.33
CPW C	0.67	0.97	1.39
CPW D	0.64	0.93	1.33
OPS_CPW A	1.03	1.56	2.06
OPS_CPW B	1.06	1.65	2.20

Table 2. Simulated conductor loss (Maxwell 2D simulation [2]) for the various circuit designs

IV. SUMMARY

The impact of biasing on various CPW architectures has been investigated. It has been shown that biasing of bare low resistivity P-type silicon (CPW C) causes a significant variation in the attenuation properties of an interconnect. However, the addition of an SiO_2 film mitigates a large part of the change. Additional improvement is observed in bias sensitivity along with reduced interconnect losses, with the use of capped porous silicon films for CPW applications. Of the porous types, porosities at 68% offer a negligible effect in bias conditions. Thus, porous silicon has the potential to offer low voltage changes in RF MEMS devices, as well as, electrically thick media for integrated antenna design on silicon substrates.

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