Advances in FDTD Acceleration

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The Finite-Difference Time-Domain (FDTD) Method has been widely and successfully applied to the modelling of complex electromagnetic behavior. The method is both flexible and accurate for a wide range of problems. The major drawback of FDTD is that it is computationally intensive and, hence, simulations can run for hours to days on multiprocessor supercomputers. Drastically reducing the runtime of FDTD simulations would greatly benefit FDTD users and open up new avenues of research. The primary goal of the research is to achieve an order of magnitude acceleration for existing FDTD software, as compared to a current personal computer (PC), by using (i) custom, programmable hardware, (ii) fine-grained parallelism and (iii) integer arithmetic. It is also desirable that this level of acceleration is achieved at a lower cost than current "accelerated" implementations.

Traditionally, FDTD has been accelerated by using parallel processing implementations, namely multi-processor, shared-memory architectures and distributed message-passing architectures. More recently, other research has been performed into hardware accelerators for FDTD. Marek, *et al*, predict a five- to nine-fold acceleration of the main FDTD update equations and PML equations, respectively, using a simulated hardware description language (HDL) design targeted for the Sparc workstation. Placidi, *et al*, describe a simulated VLSI design intended for FDTD computations on the PC platform. This work was again limited to simulation of the hardware and they predict a four-fold acceleration of the FDTD update equations.

For our research digital circuits that compute one- and two-dimensional FDTD update equations are implemented and measured on field-programmable gate-array (FPGA) hardware. Table I depicts the acceleration achieved compared to a reference PC.

TABLE I
HARDWARE ACCELERATION OF ONE- AND TWO-DIMENSIONAL FDTD

Simulation Method	Runtime† (ms)	Acceleration
Software - 1D	71	
Hardware - 1D	8.49	8.4X
Software - 2D	230	
Hardware - 2D	12.5	18.4X

†10,000 time steps

This method implements every single cell of the simulation in hardware. The computations are performed using a bit-serial, pipelined architecture and 2's-complement, integer arithmetic. A larger simulation requires more hardware, but also yields greater acceleration. Other methods are also discussed which reuse a smaller amount of hardware to achieve the desired acceleration.